General Purpose Base Board for Gate Driver Core 2SC0108T

Application	General purpose drives, UPS, solar power and others
Specification	Suitable for IGBT power modules in various housings Up to 1200V DC-link voltage Electrical interfaces Basic Active Clamping Short-circuit detection with Soft Shut Down (SSD)
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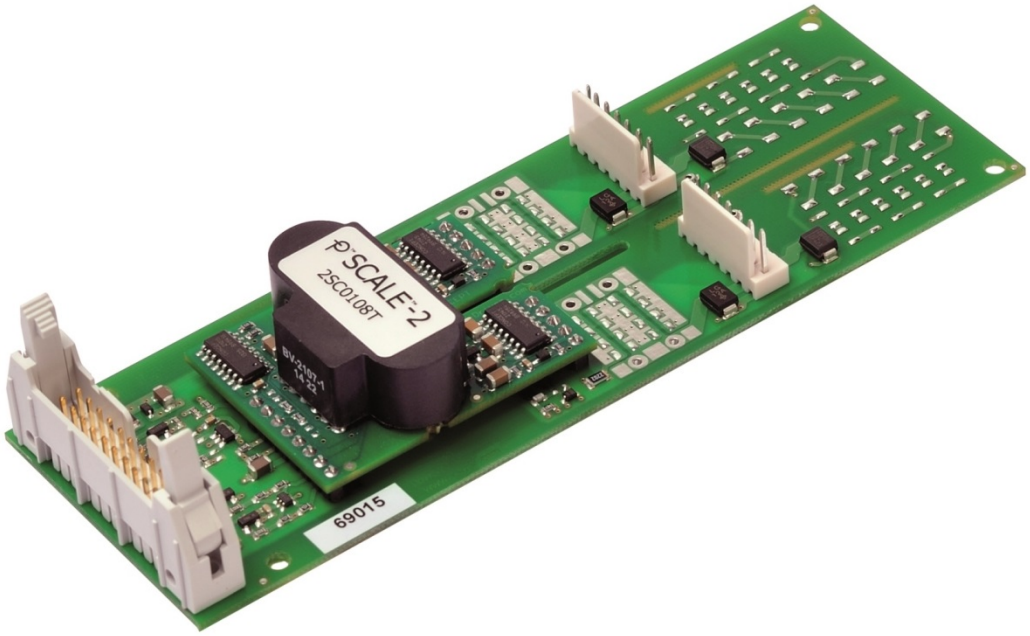

[1] The letter refers to the hardware revision. The number refers to the documentation revision.

Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 17mm dual, 17mm six-pack, 62mm, PrimePACK™, etc. with a maximum blocking voltage of 1700V
- (Optional) Basic Active Clamping
- Short-circuit detection with Soft Shut Down (SSD)
- Electrical command inputs and status outputs
- 0V/15V command input logic
- 0V/15V status output logic
- Minimum pulse suppression (optional)
- Adjustable blocking time
- 15V supply voltage
- Single PCB solution with soldered-in gate driver core

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Adaptations such as adjustment of gate resistors can easily be done

Design Description

In addition to the following design description, reference to the datasheet(s) and application manual of the 2SC0108T gate driver family is recommended.

Gate Resistors

Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR02) package can be selected.

Turn-on gate resistors:

Channel	SMD Package	THT Package
1	R118a … R118d	R116
2	R218a … R218d	R216

Turn-off gate resistors:

Channel	SMD Package	THT Package
1	R117a … R117d	R115
2	R217a … R217d	R215

The gate resistors must be determined and assembled by the user. Minimum required gate resistor values are defined in the datasheet of the gate driver 2SC0108T.

V_{CEsat} Monitoring

In the schematic and bill of material, the resistor networks of the V_{CEsat} monitoring function are marked with "N.A." (not assembled), as their concrete value depends on the IGBT power module and applied DC-link voltage.

Recommended values are listed in the following table:

IGBT voltage	Max. DC-link voltage	R101	R102 to R113	R201	R202 to R213
600V	400V	62kΩ	47kΩ	62kΩ	47kΩ
1200V	800V	120kΩ	100kΩ	120kΩ	100kΩ
1700V	1200V	120kΩ	150kΩ	120kΩ	150kΩ

Recommended values of the blanking capacitors C100 and C200 as well as further details of the V_{CEsat} monitoring function are described in the corresponding application manual of the gate driver 2SC0108T.

Soft Shut Down (SSD)

The gate driver cores 2SC0108T with SCALE-2+ chip set feature an SSD function, which reduces the turn-off $^{di}/_{dt}$ to limit V_{CE} overvoltage spikes as soon as a short-circuit condition is detected. An excessive turn-off overvoltage is therefore avoided and the IGBT is turned off within its safe operating area.

The SSD function is only active under short-circuit conditions, but not under normal operating conditions (e.g. at nominal current or in over-current conditions), i.e. it is triggered by the V_{CEsat} monitoring function.

The SSD function may also have performance limitations, such as at high DC-link voltages and/or high commutation loop stray inductances. If the application is operated at these boundary conditions, it is recommended to implement Basic Active Clamping.

For further details concerning the SSD function refer to the application manual of the gate driver core 2SC0108T.

Basic Active Clamping

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic Active Clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate.

In the schematic and bill of material the TVS networks (D103 to D108 and D203 to D208) are marked with "N.A." (not assembled) as their specific value depends on the IGBT power module and applied DC-link voltage. Recommended values are listed in the following table.

IGBT voltage	Max. DC-link voltage	D102, D202	D103 … D107, D203 … D207	D108, D208
600V	400V	STPS340U	P6SMJ70A	P6SMBJ70CA
1200V	800V	STPS340U	SMBJ130A-E3	SMBJ130CA-E3
1700V	1200V	STPS340U	P6SMB220A	P6SMB220CA

Basic Active Clamping is recommended as an additional option in case the Soft Shut Down (SSD) function of the gate driver core is used. For further details and alternative TVS diodes refer to the application manual of the gate driver core 2SC0108T.

Minimum Pulse Suppression

This design possesses the option to implement a minimum pulse suppression with a time constant τ. If required the minimum pulse suppression can be set by adjusting C300 and C301. The time constant τ is given by the following equations:

$\tau_1 = 0.88k\Omega \cdot C300$

$\tau_2 = 0.88k\Omega \cdot C301$

Recommended values of C300 and C301 are in the range of 100pF (τ_x = 88ns) to 470pF (τ_x = 414ns), depending on actual application conditions.

Blocking Time

During the blocking time the gate driver ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver's secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

The terminal TB allows the default blocking time of typically 99ms (R318) to be reduced by connecting an optional external resistor to GND. The external resistor R_b needs to be equal or larger than 129kΩ to fulfill the following formula:

$(R_b + 6.8k\Omega) \,||\, 150k\Omega \triangleq T_b + 51ms$ with $20ms < T_b < 99ms$

In case the terminal TB is directly shorted to GND ($R_b = 0\Omega$), the blocking time is set to its minimum value as descripted in the datasheet of the gate driver core 2SC0108T.

Interfaces

Electrical Interfaces

X3		
Pin	Designation	Description
1	n.c.	Not connected
3	n.c.	Not connected
5	VCC	15V supply (referenced to GND)
7	VCC	15V supply (referenced to GND)
9	SO2	Status output channel 2
11	INB	Command input channel 2
13	SO1	Status output channel 1
15	INA	Command input channel 1
17	MOD	Mode selector
19	TB	Set blocking time

X3		
Pin	Designation	Description
2	GND	Ground
4	GND	Ground
6	GND	Ground
8	GND	Ground
10	GND	Ground
12	GND	Ground
14	GND	Ground
16	GND	Ground
18	GND	Ground
20	GND	Ground

X1		
Pin	Designation	Description
1	C1	Collector channel 1
2	n.c.	Not connected
3	n.c.	Not connected
4	n.c.	Not connected
5	n.c.	Not connected
6	G1	Gate channel 1
7	VE1	Emitter channel 1

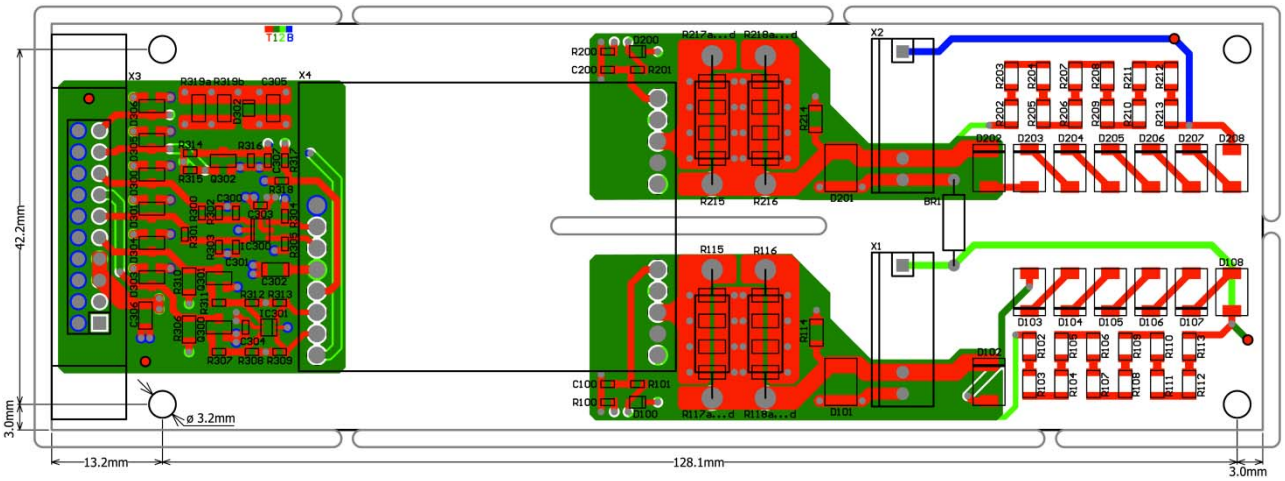
X2		
Pin	Designation	Description
1	C2	Collector channel 2
2	n.c.	Not connected
3	n.c.	Not connected
4	n.c.	Not connected
5	n.c.	Not connected
6	G2	Gate channel 2
7	VE2	Emitter channel 2

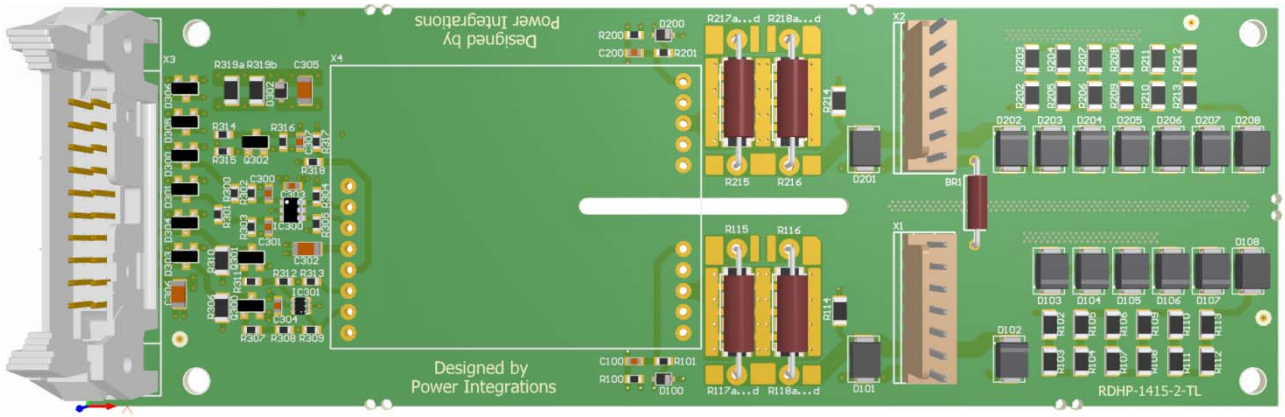
CAD Data

The set of CAD data, which includes the circuit schematics, Gerber files, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 1.55mm (for gate driver cores with terminal length of 2.54mm) and 2.0mm (for gate driver cores with terminals length ≥3.1mm).





Switching Characteristic

Turn-On / Off

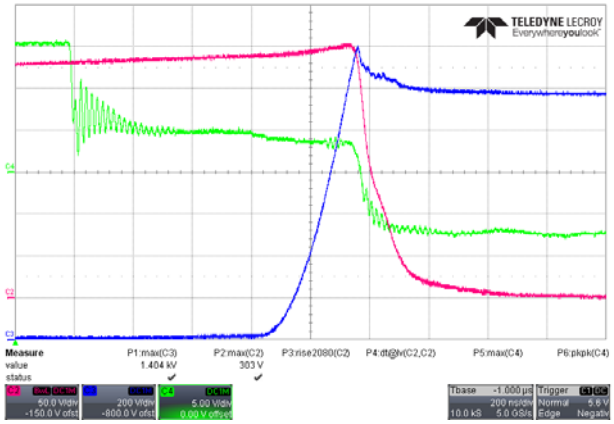
The following measurement examples were carried out at room temperature with the IGBT power module FF300R17KE3 from Infineon Technologies (R_{Gon} = 4.7Ω and R_{Goff} = 4.7Ω) in a double-pulse test using a half-bridge topology setup with an initial DC-link voltage of 1200V_{DC}. The adjusted load current is either 300A (I_{nom}) or 600A (2x I_{nom}).

Channel assignment:

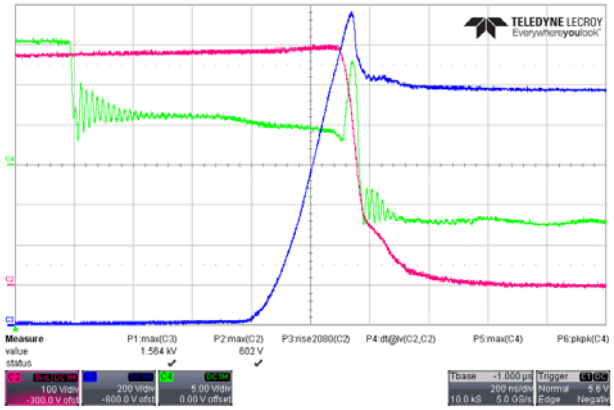
Channel C2: Collector current (1V ≙ 1A)

Channel C3: Collector-emitter voltage

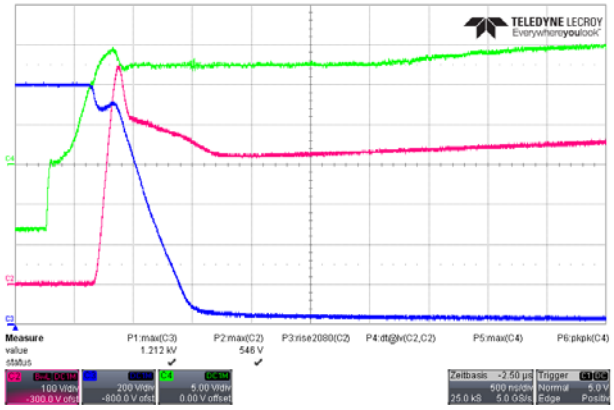
Channel C4: Gate-emitter voltage



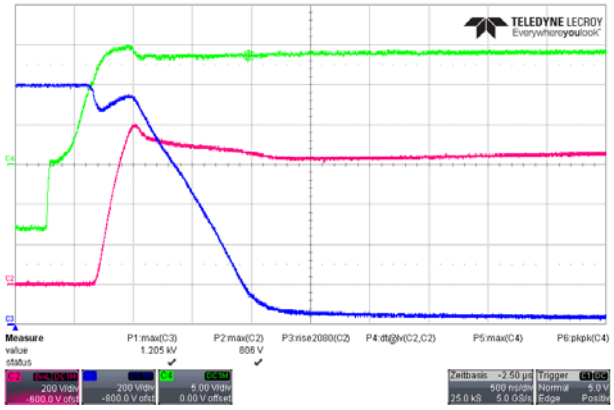
Turn-off bottom side (I_{nom})



Turn-off bottom side (2x I_{nom})



Turn-on bottom side (I_{nom})



Turn-on bottom side (2x I_{nom})

Short-Circuit

The following measurement example was carried out at room temperature with the IGBT power module FF300R17KE3 from Infineon Technologies (R_{Gon} = 4.7Ω and R_{Goff} = 4.7Ω) with an initial DC-link voltage of 1200V_{DC}.

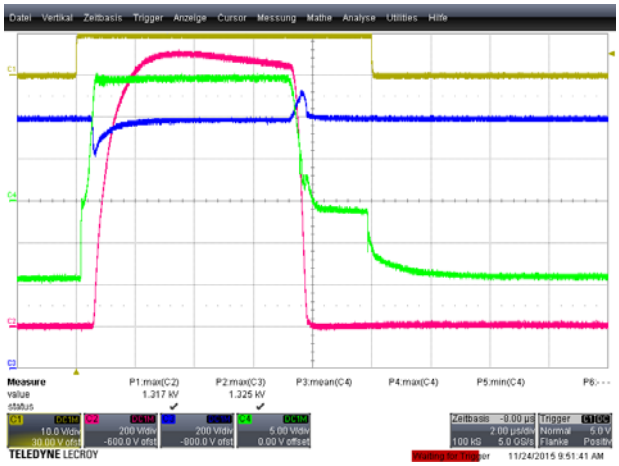
Channel assignment:

Channel C1: Command input signal

Channel C2: Collector current (1V ≙ 1A)

Channel C3: Collector-emitter voltage

Channel C4: Gate-emitter voltage



Bottom side

Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /3/.

References

/1/ 2SC0108T2xx-17 Data Sheet, Power Integrations

/2/ 2SC0108T2xx-17 Description & Application Manual, Power Integrations

/3/ Application Note AN-0902, "Avoiding ESD with CONCEPT Drivers", Power Integrations

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