

Design Example Report

Title	<i>45 W USB PD 3.0 Power Supply with 5 V / 9 V / 15 V / 20 V Output Using InnoSwitch™ 3-Pro PowiGaN™ INN3379C-H302 and VIA Labs VP302 Controller</i>
Specification	90 VAC – 265 VAC Input; 5 V / 3 A; 9 V / 3 A; 15 V / 3 A; 20 V / 2.25 A Outputs;
Application	Mobile Phone Charger
Author	Applications Engineering Department
Document Number	DER-600
Date	February 4, 2020
Revision	1.0

Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
 - I²C Interface enables low pin count USB PD Controller (8 pin)
 - Sophisticated telemetry and comprehensive protection features
- USB PD 3.0 using highly optimized, low pin count USB PD controller VP302
- All the benefits of secondary-side control with the simplicity of primary-side regulation
 - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement (>1% efficiency margin)
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- <20 mW no-load input power
- Compact design with high power density: 13.5 W/inch³ with enclosure (45 W / 1.5 in x 1.38 in x 1.61 in), 25.56 W/ inch³ without enclosure (45W/ 1.2875 in X 1.08 in X 1.266 in)

Power Integrations

5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.



Table of Contents

1	Introduction.....	6
2	Power Supply Specification	9
3	Schematic.....	10
4	Circuit Description	12
4.1	Input Rectifier and EMI Filter.....	12
4.2	InnoSwitch3-Pro IC Primary	12
4.3	InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller	12
5	PCB Layout.....	15
6	Bill of Materials	18
7	Transformer Specification	20
7.1	Electrical Diagram.....	20
7.2	Electrical Specifications	20
7.3	Material List	20
7.4	Transformer Build Diagram	21
7.5	Transformer Construction.....	22
7.6	Winding Illustrations	23
8	Common Mode Choke Specifications	30
8.1	630 μ H Common Mode Choke (L1)	30
8.1.1	Electrical Diagram	30
8.1.2	Electrical Specifications.....	30
8.1.3	Material List.....	30
8.1.4	Common Mode Choke Construction.....	31
9	Transformer Design Spreadsheet	32
10	PCB Assembly Instructions	35
10.1	Material List	35
10.2	Capacitors Assembly Taping Instructions.....	35
10.2.1	Output Capacitor C12 and C20 Taping Instructions	35
10.2.2	Bulk Capacitor C2 Taping Instructions	37
10.2.3	Bias Capacitor Taping Instructions	38
10.2.4	Y Capacitor Sleeving Instructions	39
10.3	Daughter Boards Assembly Instructions	40
11	Adapter Case and Thermal Pad Assembly	43
11.1	Material List	43
11.2	Adapter Case Dimensions.....	43
11.2.1	Case Body	43
11.2.2	Case Cap.....	44
11.3	Thermal Pad Dimensions.....	44
11.3.1	Thermal Pad	44
11.4	Thermal Pad and Case Assembly Illustrations	45
12	Performance Data	47
12.1	No-Load Input Power at 5 V_{OUT}	47
12.2	Average and 10% Load Efficiency.....	47
12.2.1	Efficiency Requirements	47

12.2.2	Efficiency Performance Summary (On Board).....	47
12.2.3	Average and 10% Load Efficiency at 115 VAC.....	48
12.2.4	Average and 10% Load Efficiency at 230 VAC.....	49
12.3	Efficiency Across Load (On Board)	50
12.3.1	Output: 5 V / 3 A	50
12.3.2	Output: 9 V / 3 A.....	51
12.3.3	Output: 15 V / 3 A	52
12.3.4	Output: 20 V / 2.25 A.....	53
12.4	Efficiency Across Line (On Board)	54
12.5	Load Regulation (On Board)	55
12.5.1	Output: 5 V / 3 A	55
12.5.2	Output: 9 V / 3 A	56
12.5.3	Output: 15 V / 3 A	57
12.5.4	Output: 20 V / 2.25 A.....	58
12.6	Line Regulation (On Board)	59
12.6.1	Output: 5 V / 3 A	59
12.6.2	Output: 9 V / 3 A	60
12.6.3	Output: 15 V / 3 A	61
12.6.4	Output: 20 V / 2.25 A.....	62
13	Thermal Performance.....	63
13.1	Thermal Performance with Adapter Case Enclosure	63
13.1.1	Output: 20 V / 2.25 A (90 VAC /265 VAC), Ambient Temperature: 25 °C..	63
13.1.2	Output: 15 V / 3 A (90 VAC /265 VAC), Ambient Temperature: 25 °C.....	63
13.1.3	Output: 20 V / 2.25 A (90 VAC /265 VAC), Ambient Temperature: 40 °C..	63
13.1.4	Output: 15 V / 3 A (90 VAC /265 VAC), Ambient Temperature: 40 °C.....	64
14	Waveforms.....	65
14.1	Start-up Waveforms.....	65
14.1.1	Output Voltage and Current.....	65
14.1.2	Primary Drain Voltage and Current.....	65
14.1.3	SR FET Drain Voltage and Load Current	66
14.2	Load Transient Response	67
14.2.1	Output: 5 V / 3 A	67
14.2.2	Output: 9 V / 3 A	67
14.2.3	Output: 15 V / 3 A	68
14.2.4	Output: 20 V / 2.25 A.....	68
14.3	Primary Drain Voltage and Current (Steady-State)	69
14.3.1	Output: 5 V / 3 A	69
14.3.2	Output: 9 V / 3 A	69
14.3.3	Output: 15 V / 3 A	70
14.3.4	Output: 20 V / 2.25 A.....	70
14.4	SR FET Drain Voltage and Load Current (Steady-State).....	71
14.4.1	Output: 5 V / 3 A	71
14.4.2	Output: 9 V / 3 A	71
14.4.3	Output: 15 V / 3 A	72



14.4.4	Output: 20 V / 2.25 A.....	72
15	Output Ripple Measurements.....	73
15.1	Ripple Measurement Technique.....	73
15.2	Output Voltage Ripple Waveforms.....	74
15.2.1	Output: 5 V / 3 A.....	74
15.2.2	Output: 9 V / 3 A.....	75
15.2.3	Output: 15 V / 3 A.....	76
15.2.4	Output: 20 V / 2.25 A.....	77
15.2.5	Output: 5 V / 0 A.....	78
15.2.6	Output: 9 V / 0 A.....	79
15.2.7	Output: 15 V / 0 A.....	80
15.2.8	Output: 20 V / 0 A.....	81
16	Conducted EMI.....	82
16.1	Floating Ground (QPK / AV).....	82
16.1.1	Output: 5 V / 3 A.....	82
16.1.2	Output: 9 V / 3 A.....	83
16.1.3	Output: 15 V / 3 A.....	84
16.1.4	Output: 20 V / 2.25 A.....	85
17	Combination Wave Surge.....	86
17.1	Differential Mode Surge (L1 to L2), 230 VAC Input.....	86
17.2	Common Mode Surge (L1 to PE), 230 VAC Input.....	86
17.3	Common Mode Surge (L2 to PE), 230 VAC Input.....	86
17.4	Common Mode Surge (L1, L2 to PE), 230 VAC Input.....	87
18	Electrostatic Discharge.....	88
18.1	Contact Discharge, 230 VAC input.....	88
18.2	Air Discharge, 230 VAC input.....	88
19	Revision History.....	89

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 45 W USB PD power supply with 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 2.25 A, output using InnoSwitch3-Pro INN3379-H302 IC and VIA Labs VP302 USB PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-Pro controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics and adapter case specifications, and performance data.

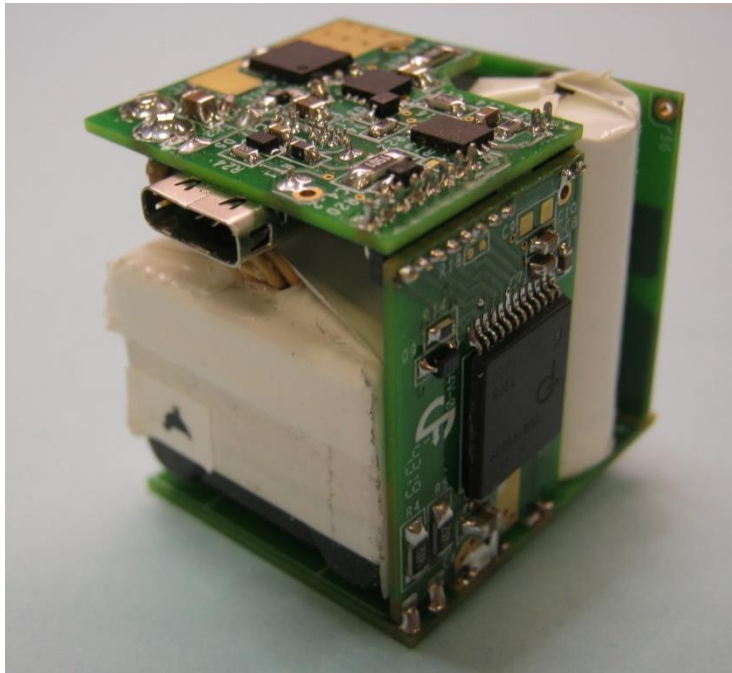


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

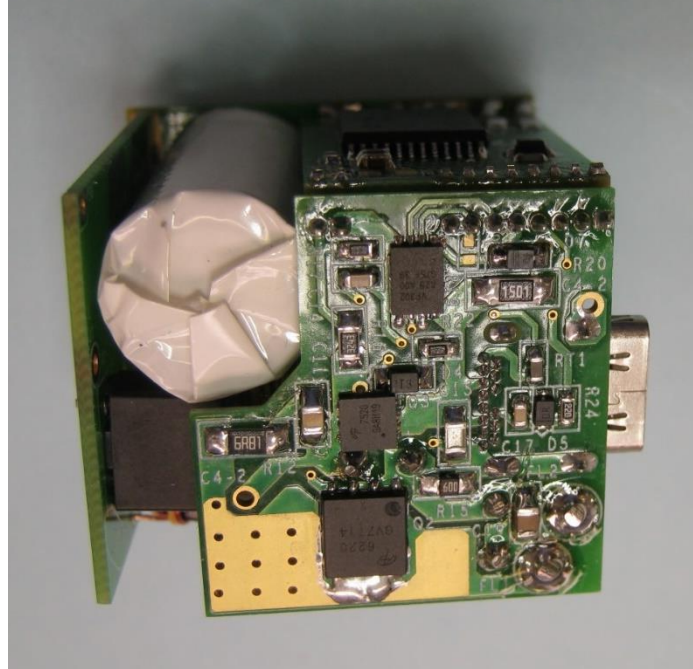


Figure 2 – Populated Circuit Board Photograph - Top.

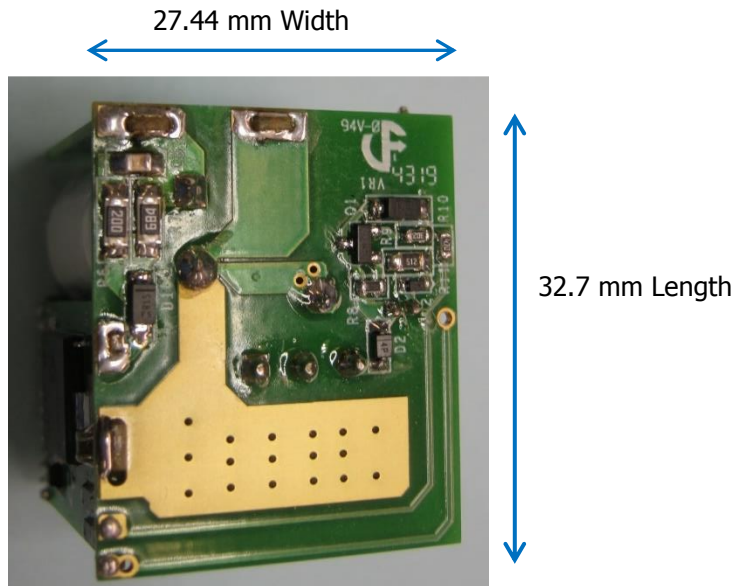


Figure 3 – Populated Circuit Board Photograph - Bottom.

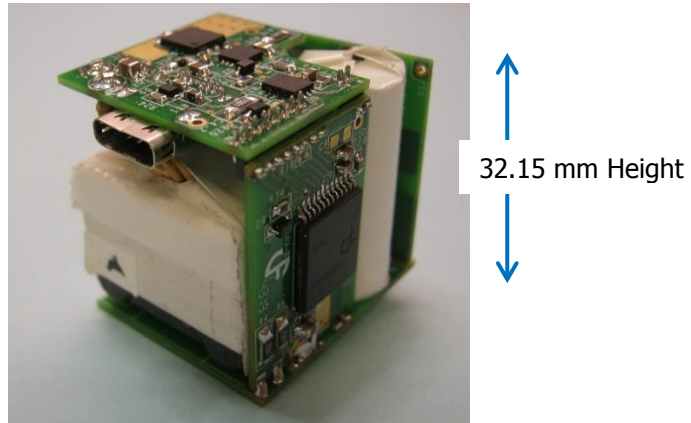


Figure 4 – Populated Circuit Board Photograph - Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				15.4	mW	Measured at 230 VAC.
5 V Setting						
Output Voltage	$V_{OUT(5V)}$		5.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(5V)}$			300	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(5V)}$			3.0	A	±3%
Average Efficiency	$\eta(5V)$		>91		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(5V)}$			15	W	
9 V Setting						
Output Voltage	$V_{OUT(9V)}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(9V)}$			250	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(9V)}$			3.0	A	±3%
Average Efficiency	$\eta(9V)$		>92		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(9V)}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT(15V)}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(15V)}$			250	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth)..
Output Current	$I_{OUT(15V)}$			3.0	A	±3%
Average Efficiency	$\eta(15V)$		>92		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(15V)}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT(20V)}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE(20V)}$			250	mV	Measured at End of 100 mΩ Cable. (20 MHz Bandwidth).
Output Current	$I_{OUT(20V)}$			2.25	A	±3%
Average Efficiency	$\eta(20V)$		>92		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT(20V)}$			45	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Note: To use this design for a charger/adapter, circuit board would need to be modified depending on shape and form factor of the housing. ESD and Line surge performance should be evaluated and layout adjusted to meet the target specification.

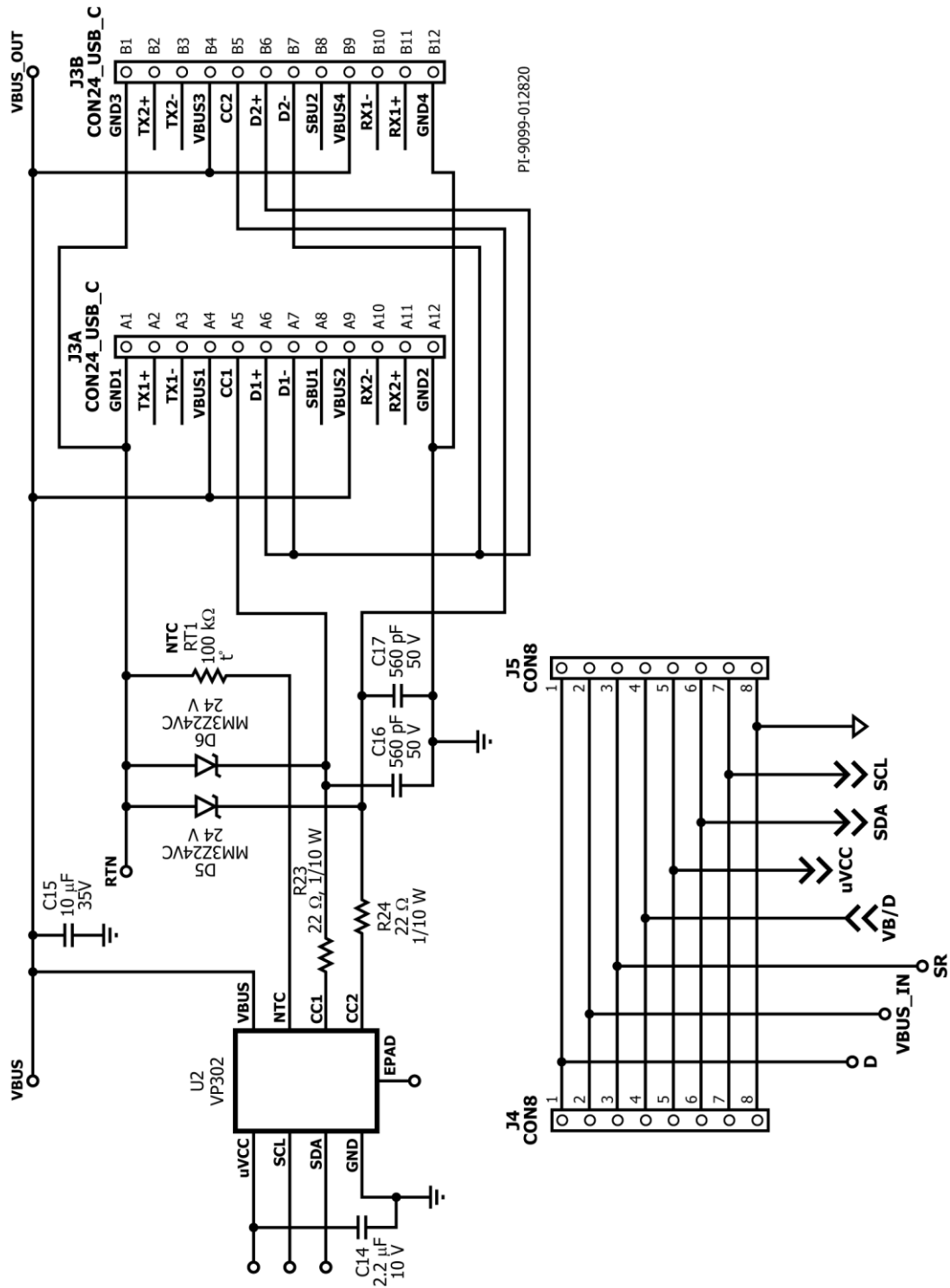


Figure 6 – Schematic, USB PD Controller Section.

Note:

Component references R1, R2, R18, R19, R20, R21, D7, D8, and C9, although present in the layout, should not be populated.



4 Circuit Description

4.1 Input Rectifier and EMI Filter

Fuse F1 isolates the circuit and provides protection from component failure. Differential mode choke L1 and Common mode choke L2, with capacitors C1 and C4 provide differential mode and common mode noise filtering for EMI attenuation. Bridge rectifier formed by BR1 rectifies the AC line voltage and provides a full wave rectified DC across C2.

4.2 InnoSwitch3-Pro IC Primary

One end of the transformer primary is connected to the rectified DC bus and the other end is connected to the drain terminal of the switch inside the InnoSwitch3-Pro IC U1. Resistors R4 and R5 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost RCD clamp formed by diode D1, resistors R6, R7, and capacitor C3 limits the peak drain-source voltage of U1 at the instant the switch inside U1 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C6 when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R10 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC U1. A linear regulator comprising resistor R8, R9, BJT Q1 and Zener diode VR2 ensures sufficient current flows through R10 such that the internal current source of U1 is not required to charge C6 during normal operation.

Zener diode VR1 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes excess current to flow into the BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage. Resistor R11 limits the current injected to BPP pin during output overvoltage protection event.

4.3 InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing and a gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side FET (or SR FET) Q2 and filtered by capacitor C12 and C20. High frequency ringing during switching transients that

would otherwise create radiated EMI is reduced via a RCD snubber, R12, R13, C11, and D3.

The gate of Q2 is turned on by secondary-side controller inside IC U1, based on the secondary winding voltage sensed via resistor R14 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C7 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R15. Resistors R16 and R17 add an offset to the sensed output current to provide a positive slope to the CC characteristic. The resulting current measurement is filtered with decoupling capacitor C8 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the I²C interface up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-Pro IC U1 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary-side controller inside InnoSwitch3-Pro IC U1 will power itself from the secondary winding directly. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C7 via resistor R14 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the I²C interface and the controller inside IC U1 regulates the output voltage by controlling the number of switch pulses. Capacitor C9 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-channel MOSFET Q3 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. N-channel MOSFET Q3

is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R22 and diode D4 are connected across the Source and Gate terminals of the Q3 to provide a discharge path for the bus voltage when the Q3 is turned off. Capacitors C15 and C21 are used at the output for ESD protection.

In this design, VP302 (U2) is the USB Power Delivery (USB PD) controller. It is powered by the InnoSwitch3-Pro IC through the μ VCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

The VP302 IC communicates with InnoSwitch3-Pro IC through the I²C interface using the SCL and SDA lines in which it sets the CV, CC, V_{KP} , OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the VP302 IC from the telemetry registers also using the I²C interface.

Capacitors C10 and C14 provide decoupling to the μ VCC of the InnoSwitch3-Pro IC and VCC of the VP302 IC. Capacitors C16 and C17, resistors R23 and R24, and TVS diodes D5, and D6 provide protection from ESD to pins CC1 and CC2.

Thermistor RT1 is connected to NTC pin of the VP302 IC to provide temperature detection of the USB Type-C receptacle. The VBUS pin of the VP302 IC is used to sense the output voltage at the USB Type-C receptacle, which is the voltage after the bus switch Q3. The VBUS pin is also used for discharging capacitor C15 when the bus switch Q3 is opened.

5 PCB Layout

PCB copper thickness is 0.062 inches.

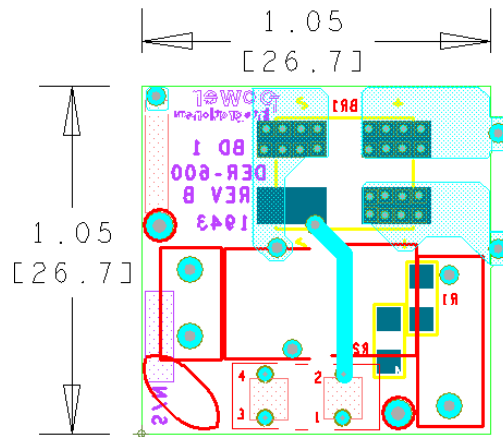


Figure 7 – Input Section Daughterboard Printed Circuit Layout, Top.

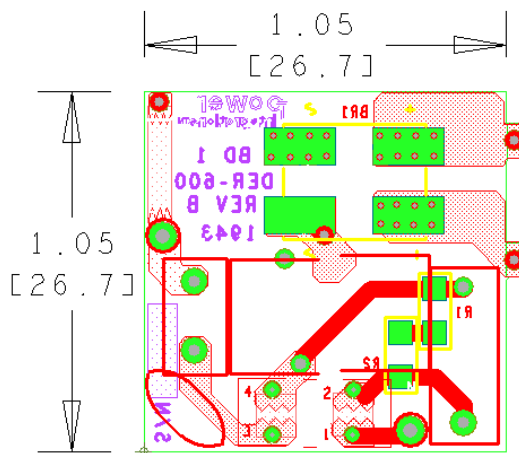


Figure 8 – Input Section Daughterboard Printed Circuit Layout, Bottom.

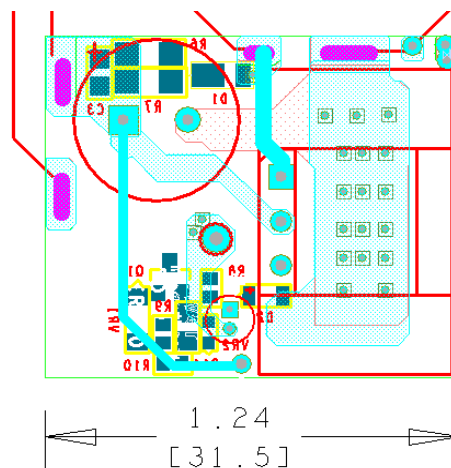


Figure 9 – Motherboard Printed Circuit Layout, Top.

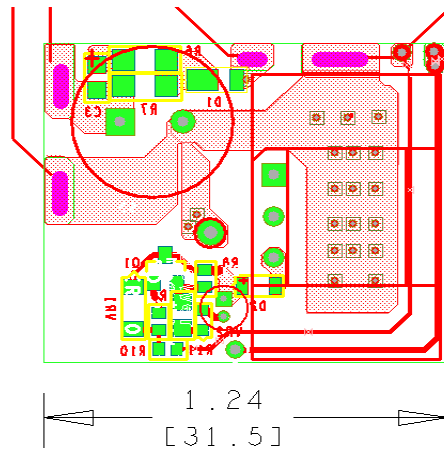


Figure 10 – Motherboard Printed Circuit Layout, Bottom.

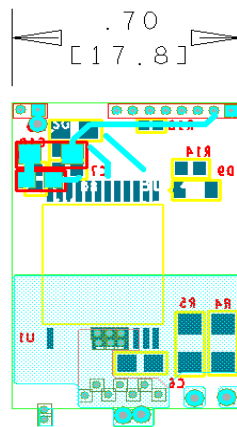


Figure 11 – InnoSwitch3-Pro Daughterboard Printed Circuit Layout, Top.

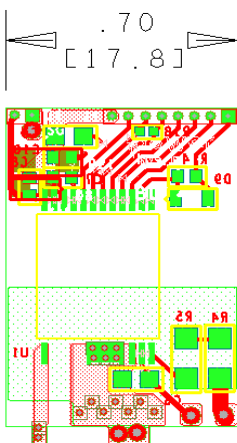


Figure 12 – InnoSwitch3-Pro Daughterboard Printed Circuit Layout, Bottom.

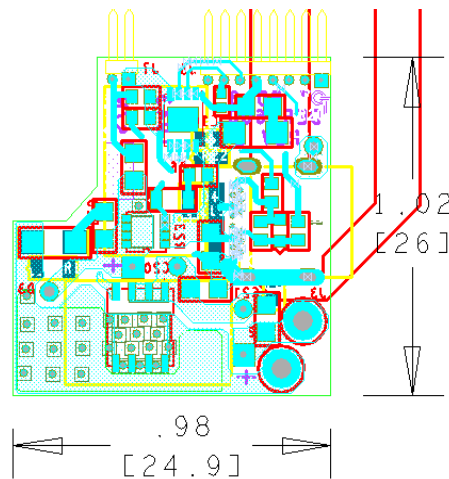


Figure 13 – USB Type-C Daughterboard Printed Circuit Layout, Top.

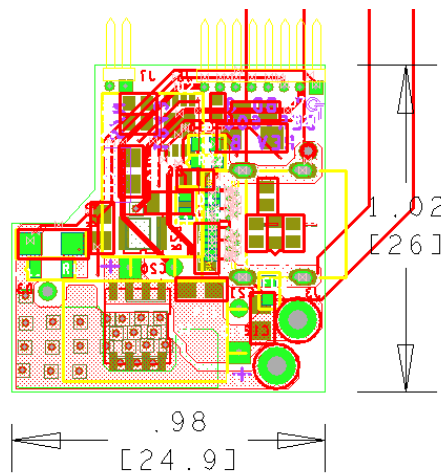


Figure 14 – USB Type-C Daughterboard Printed Circuit Layout, Bottom.

Note:

Component references R1, R2, R18, R19, R20, R21, D7, D8, and C9, although present in the layout, should not be populated.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 800 V, 4A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	0.1 μ F, 20%, 275 VAC, 560VDC, X2	R46KF310000P1M	KEMET
3	1	C2	56 μ F, 450 V, Electrolytic, (12.5 x 25)	400HXW56MEFR12.5X25	Rubycon
4	1	C3	2.2 nF, 250 V, Ceramic, X7R, 0805	C2012X7R2E222K085AA	TDK
5	1	C4	1 nF, Ceramic, Y1	440LD10-R	Vishay
6	1	C5	6.8 μ F, \pm 20%, 63 V, Electrolytic, Gen Purpose, (4 mm x 11 mm)	UPW1J6R8MDD6	Nichicon
7	1	C6	4.7 μ F, \pm 10%, 25 V, Ceramic, X7R, -55°C ~ 125°C, 0805	TMK212AB7475KG-T	Taiyo Yuden
8	3	C7 C10 C14	2.2 μ F, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
9	1	C8	4.7 μ F, 10 V, Ceramic, X5R, 0603	C1608X5R1A475M/0.50	TDK
10	1	C9	3.3 μ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E335K	TDK
11	1	C11	3.3 nF, 200 V, Ceramic, X7R, 0805	08052C332KAT2A	AVX
12	2	C12 C20	330 μ F, \pm 20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 m Ω , 2000 Hrs @ 105°C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
13	1	C15	10 μ F, 35 V, Ceramic, X5R, 0805	C2012X5R1V106K085AC	TDK
14	2	C16 C17	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60 mm x 0.80 mm)	CL10B561KB8NNNC	Samsung
15	1	C19	2.2 μ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
16	1	C21	1 μ F, \pm 10%, 35V, Ceramic, X7R, 0603	C1608X7R1V105K080AE	TDK
17	1	D1	800 V, 1 A, Fast Recovery Rectifier, POWERDI123	DFLF1800-7	Diodes, Inc.
18	1	D2	Diode, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
19	2	D3 D9	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
20	1	D4	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
21	2	D5 D6	DIODE, ZENER, 24V, 200MW, SC-90, SOD-323F	MM3Z24VC	ON Semi
22	2	D7 D8	Diode, Low Leakage, 85 V, 200 mA, SOD323	BAS416,115	NXP Sem
23	1	F1	3.15 A, 250V, Slow, RST	507-1181	Belfuse
24	1	L1	150 μ H, 20%, 2.5 A, Rdc=0.01, Inductor, TOROID, HI AMP, VERT, 16.5 mm Diam, 8.5 mm Thick, 8.5 mm LS	7447018	Würth
25	1	L2	630 μ H, Toroidal CMC, custom, wound on 32-00275-00 core	32-00397-00	Power Integrations
26	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
27	1	Q2	MOSFET, N-CH, 100 V, 48A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
28	1	Q3	MOSFET, N-CH, 30V, 45A (Ta), 75A (Tc), 4.1W (Ta), 46W (Tc), 8-DFN-EP (3.3x3.3), 8-PowerWDFN	AON7510	Alpha & Omega Semi
29	2	R4 R5	RES, 2.00 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
30	1	R6	RES, 20 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
31	1	R7	RES, 680 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
32	1	R8	RES, 100 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
33	1	R9	RES, 5.1 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ512V	Panasonic
34	1	R10	RES, 3 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
35	1	R11	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
36	2	R12 R13	RES, 6.81 Ω , 1%, 1/4 W, Thick Film, 1206	RC1206FR-076R81L	Yageo
37	1	R14	RES, 910 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ911V	Panasonic
38	1	R15	RES, 0.009 Ω , \pm 1%, 0.5 W, 0805, Current Sense, Moisture Resistant, Metal Element	CRF0805-FZ-R009ELF	Bourns
39	1	R16	RES, 324 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3243V	Panasonic
40	1	R17	RES, 10 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
41	2	R20 R21	RES, 1.5 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1501V	Panasonic
42	1	R22	RES, 100 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic



43	2	R23 R24	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
44	1	RT1	NTC Thermistor, 100 k Ω , 3%, 0603	NCP18WF104E03RB	Murata
45	1	T1	Bobbin, ATQ23.7/14, Horizontal, 4 pins. Mates with core 99-00072-00.		
46	1	U1	InnoSwitch3-Pro, InSOP24D	INN3379C-H302	Power Integrations
47	1	U2	IC, USB PD Type-C Controller for SMPS, DFN-8	VP302	VIA Labs
48	1	VR1	DIODE ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi
49	1	VR2	10 V, 5%, 150 mW, SSMINI-2,SC-79, SOD-523,EMD2	EDZVT2R10B	Rohm Semi



7 Transformer Specification

7.1 Electrical Diagram

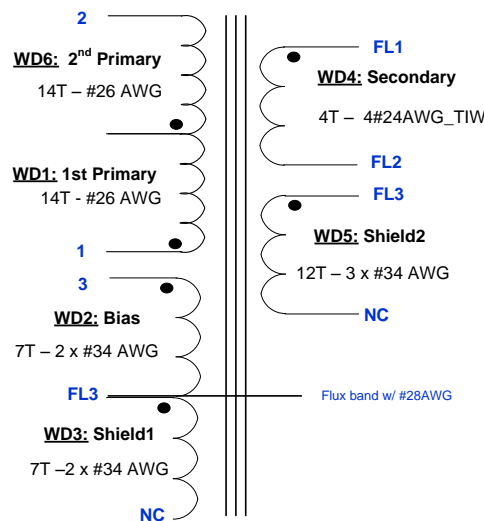


Figure 15 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Electrical Strength	1 second, 60 Hz, from pins 1-2 to FL1-FL2.	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100kHz, 0.4V _{RMS} .	425 μH, ±5%
Resonant Frequency	Pins 1-2, all other open.	2,000 kHz (Min.)
Primary Leakage	Pins 1-2, with FL1-FL2 shorted, measured at 100 kHz.	4.0 μH (Max.)

7.3 Material List

Item	Description
[1]	Core: ATQ23.7-14, PI# 99-00072-00: or equivalent. Gapped ALG: 540nH/T ² .
[2]	Bobbin: ATQ23.7-14, Horizontal, 3pins (3/0), PI#: 25-01171-00; or equivalent. (be modified as instruction below).
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 6.5 mm Wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 27.5 mm x 54.0 mm.
[8]	Copper Tape: 2mil Thick x 8.0 mm; or Equivalent.
[9]	Varnish: Dolph BC-359; or Equivalent.
[10]	Epoxy: Devcon, 5 mins Epoxy, Mfr#: 14270; or Equivalent.
[11]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

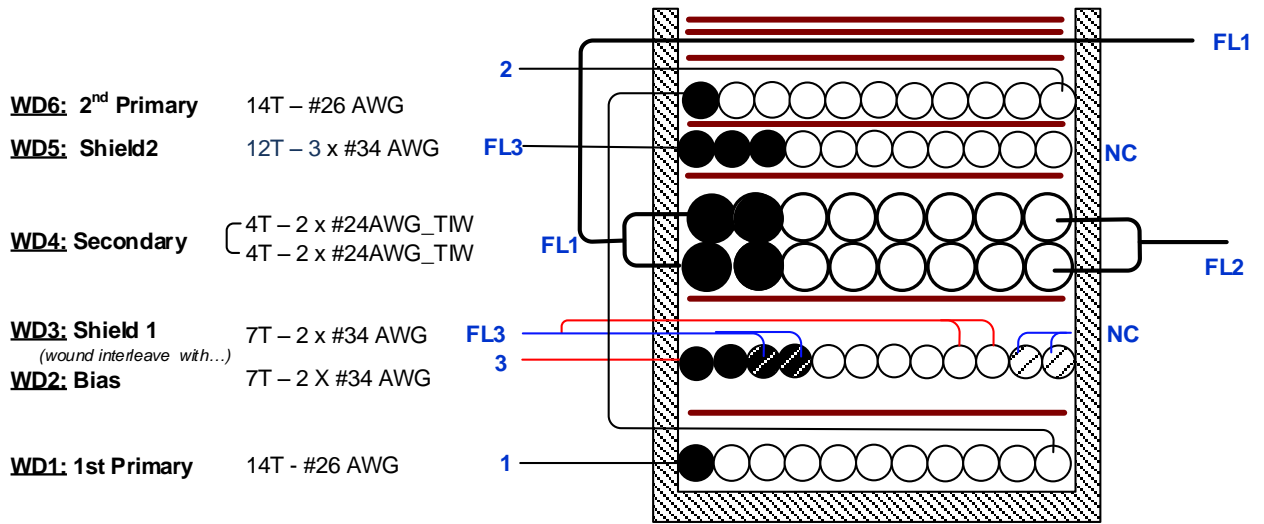


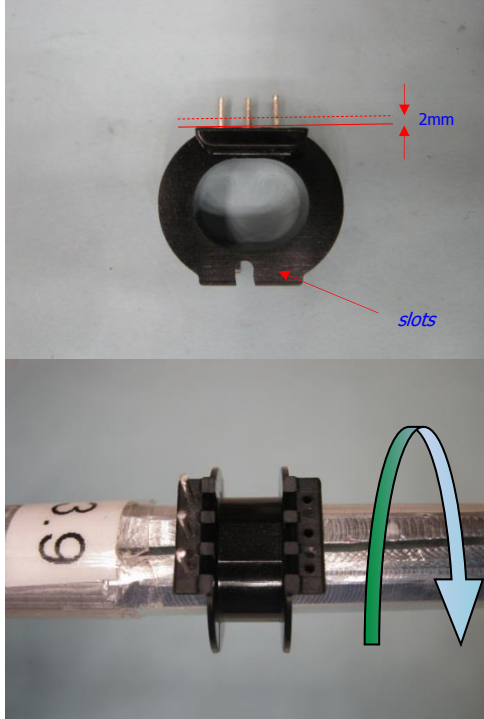
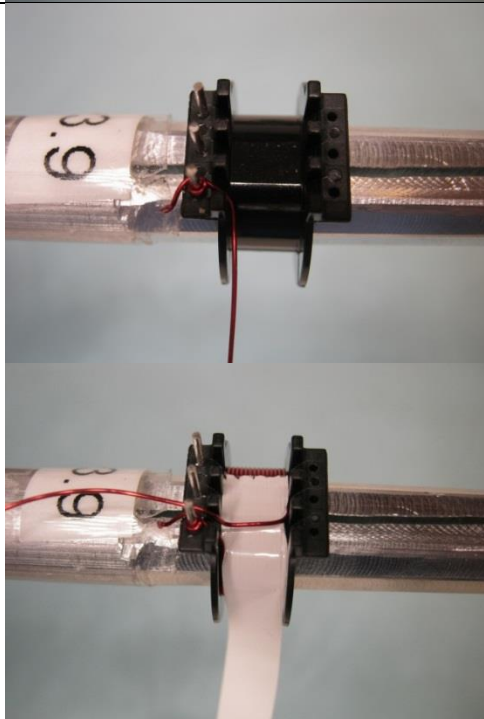
Figure 16 – Transformer Build Diagram.

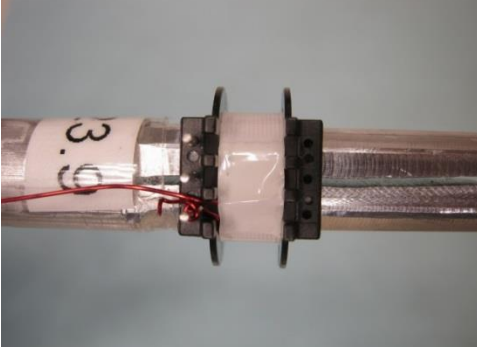
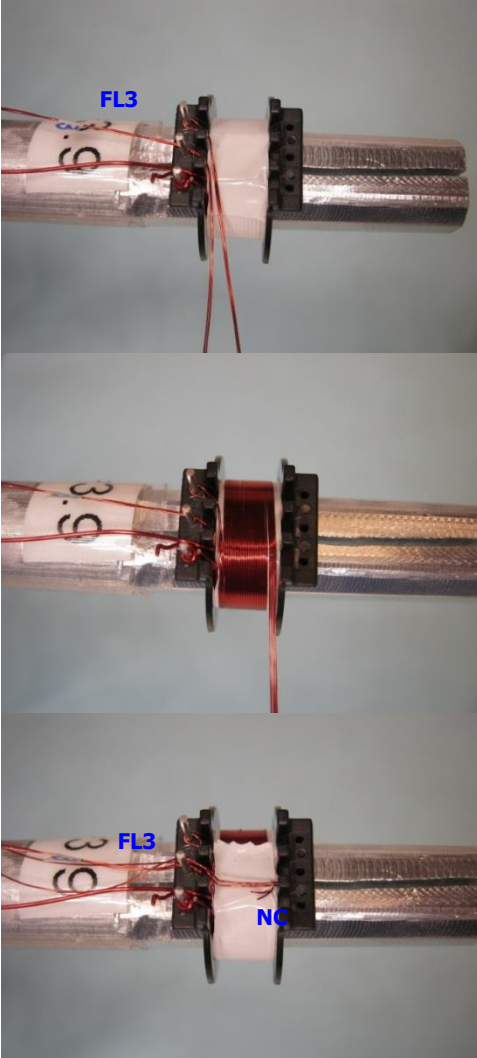


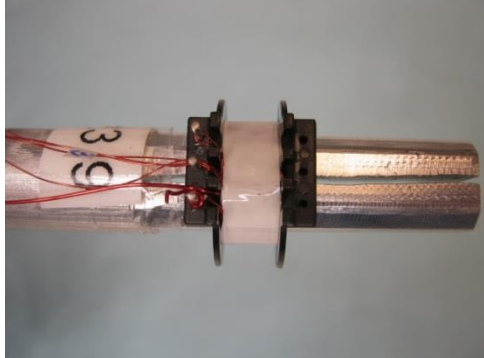
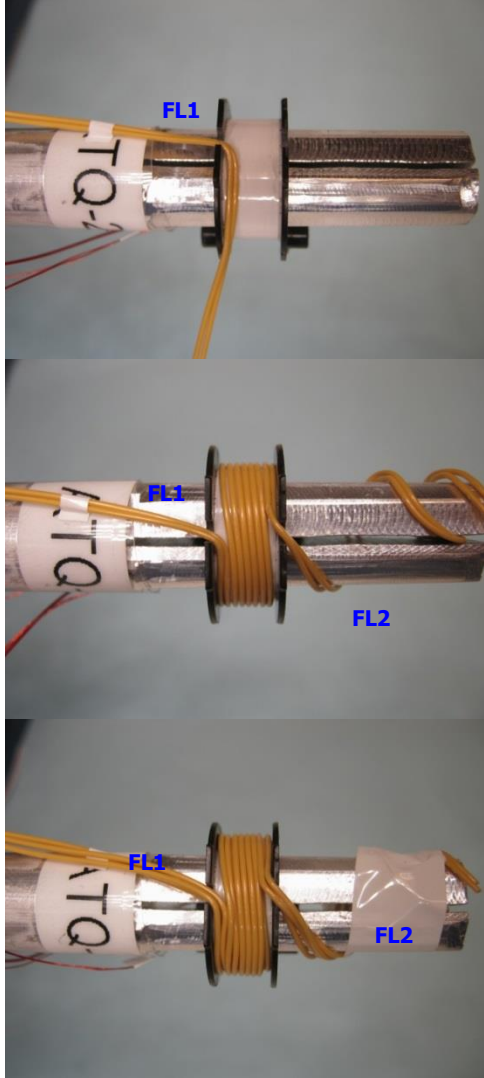
7.5 Transformer Construction

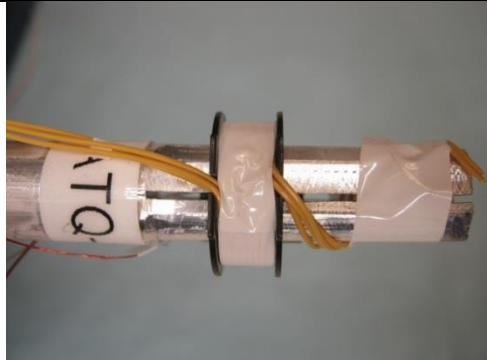
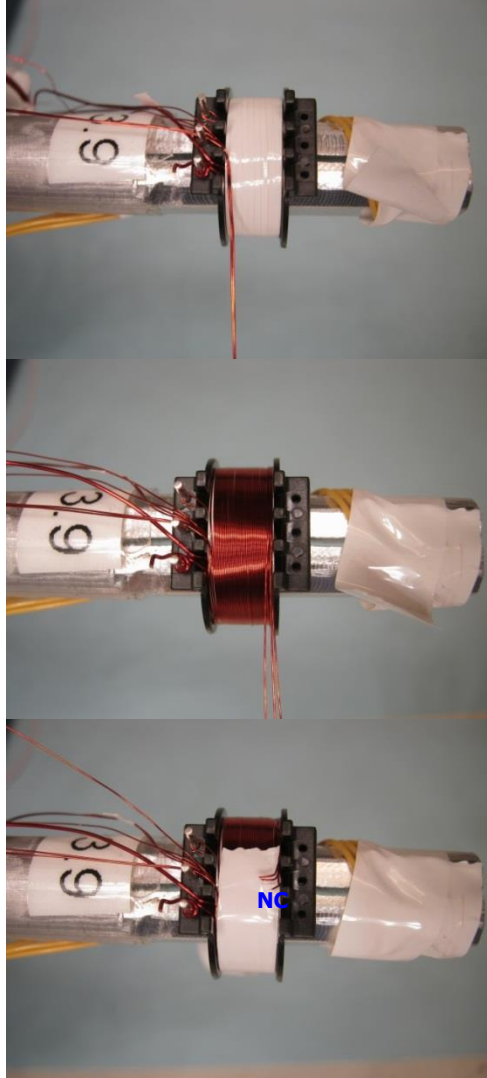
Winding Preparation	<p>Modify bobbin Item [2] as below:</p> <ul style="list-style-type: none"> - insert and remove pins of bobbin to make primary-side with 3 pins and secondary-side without pins. - trim notches down ~2 mm on both sides. - make 2 slots with ~2 mm width on both flanges of secondary-side. (<i>see illustration below</i>). <p>Now position the bobbin on the mandrel such that the pin side of the bobbin is on the left side.</p> <p>Winding direction is clock-wise direction for forward direction.</p>
WD1: 1st Primary	Start at pin 1, wind 14 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn bring the wire back to the left and leave enough length for 2 nd Primary winding-WD6.
Insulation	1 layer of tape Item [6].
WD2: Bias & WD3: Shield1	Use 2 wires Item [4] start at pin 3 for Bias winding, also use 2 wires same Item [4] start as FL3 for Shield1 winding. Wind all 4 wires in parallel, at the 7 th turn: <ul style="list-style-type: none"> - bring 2 wires for Bias winding to the left and terminate as FL3, - cut short 2 wires for Shield1 Winding as No-Connect.
Insulation	1 layer of tape Item [6].
WD4: Secondary	Start at left slot of secondary-side, use 2 wires Item [5], leaving ~40.0 mm floating, and mark as FL1. Wind 4 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~30.0 mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.
Insulation	1 layer of tape Item [6].
WD5: Shield2	Start as FL3, wind 12 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [6].
WD6: 2nd Primary	Use floating wire from WD1-1 st Primary, wind 14 turns from right to left. At the last turn, bring the wire back to left, and finish at pin 2.
Finish	<p>Place 1 layer of tape Item [6], bring the wires FL1 from secondary winding to the right at top slot of secondary-side of bobbin, and continue place 2 layers of tape.</p> <p>Gap cores to get 425 μH and secure with tape.</p> <p>Make flux band by using copper tape Item [8] which solder joint is off center and solder with wire Item [3] connect with FL3.</p> <p>Place 1 layer of tape to cover flux band.</p> <p>Varnish with Item [9].</p> <p>Place 2 layers of tape Item [7] at bottom core of transformer and wrap up to body of transformer then wrap 1 turn of tape Item [7] around the body of transformer, (<i>see illustration below</i>).</p>

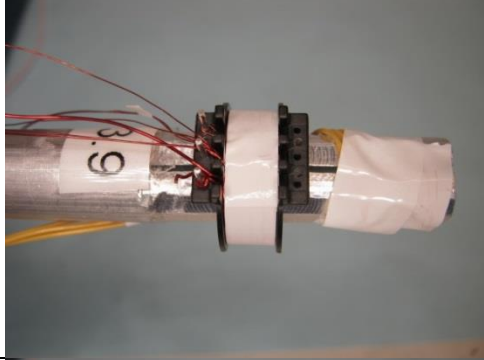
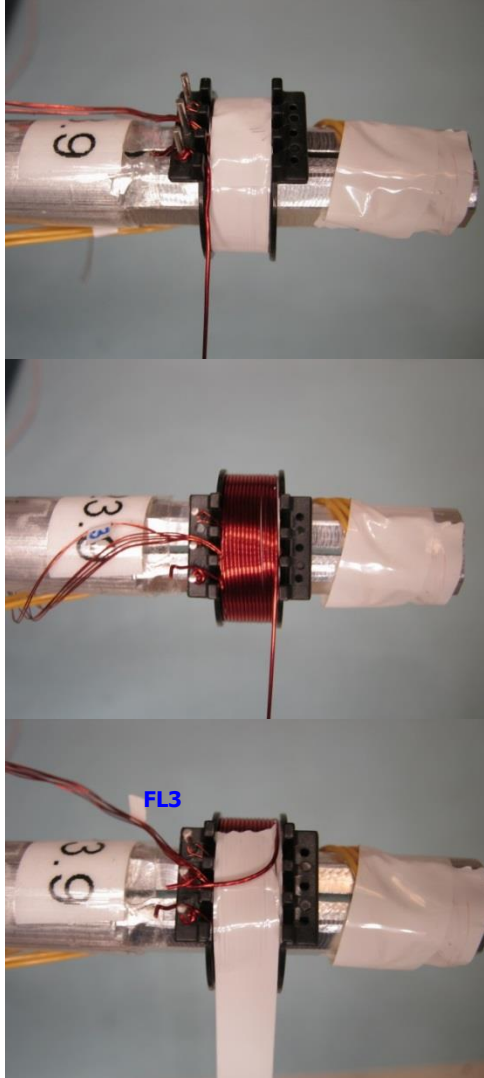
7.6 Winding Illustrations

<p>Winding Preparation</p>		<p>Modify bobbin Item [2] as below:</p> <ul style="list-style-type: none"> - insert and remove pins of bobbin to make primary-side with 3 pins and secondary-side without pins . - trim notches down ~2 mm on both sides. - make 2 slots with ~2 mm width on both flanges of secondary-side. (<i>see pics beside</i>). <p>Now position the bobbin on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.</p>
<p>WD1 1st Primary</p>		<p>Start at pin 1, wind 14 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn bring the wire back to the left and leave enough length for 2nd Primary winding-WD6.</p>

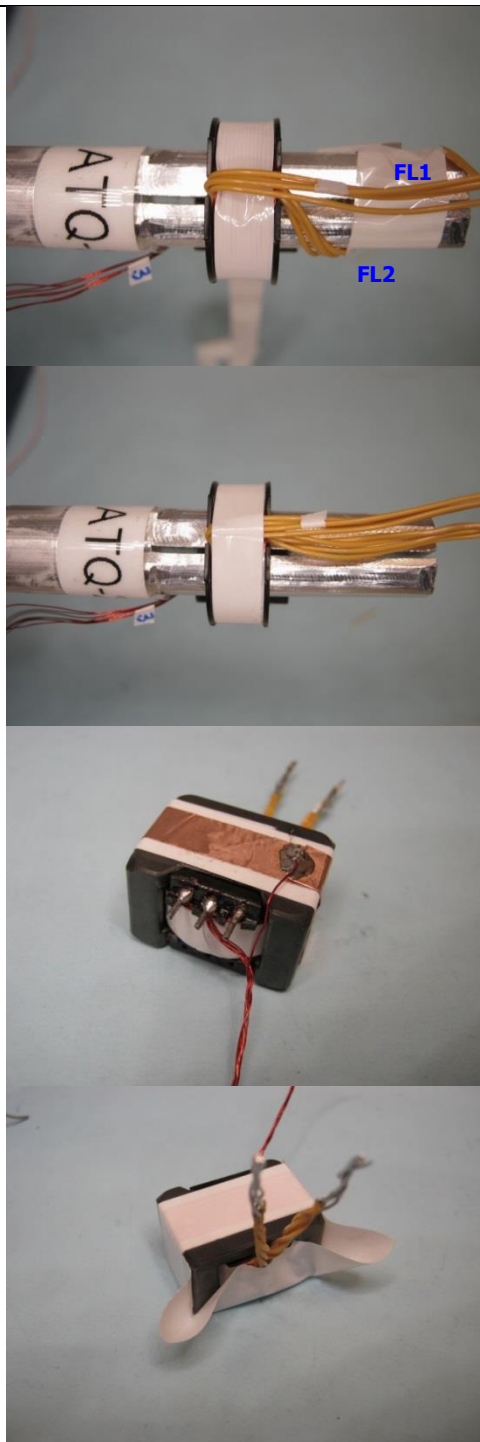
<p>Insulation</p>		<p>1 layer of tape Item [6].</p>
<p>WD2: Bias & WD3: Shield1</p>		<p>Use 2 wires Item [4] start at pin 3 for Bias winding, also use 2 wires same Item [4] start as FL3 for Shield1 winding. Wind all 4 wires in parallel, at the 7th turn:</p> <ul style="list-style-type: none">- bring 2 wires for Bias winding to the left and terminate as FL3,- cut short 2 wires for Shield1 Winding as No-Connect.

<p>Insulation</p>		<p>1 layer of tape Item [6].</p>
<p>WD4 Secondary</p>		<p>Start at left slot of secondary-side, use 2 wires Item [5], leaving ~40.0 mm floating, and mark as FL1. Wind 4 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~30.0 mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.</p>

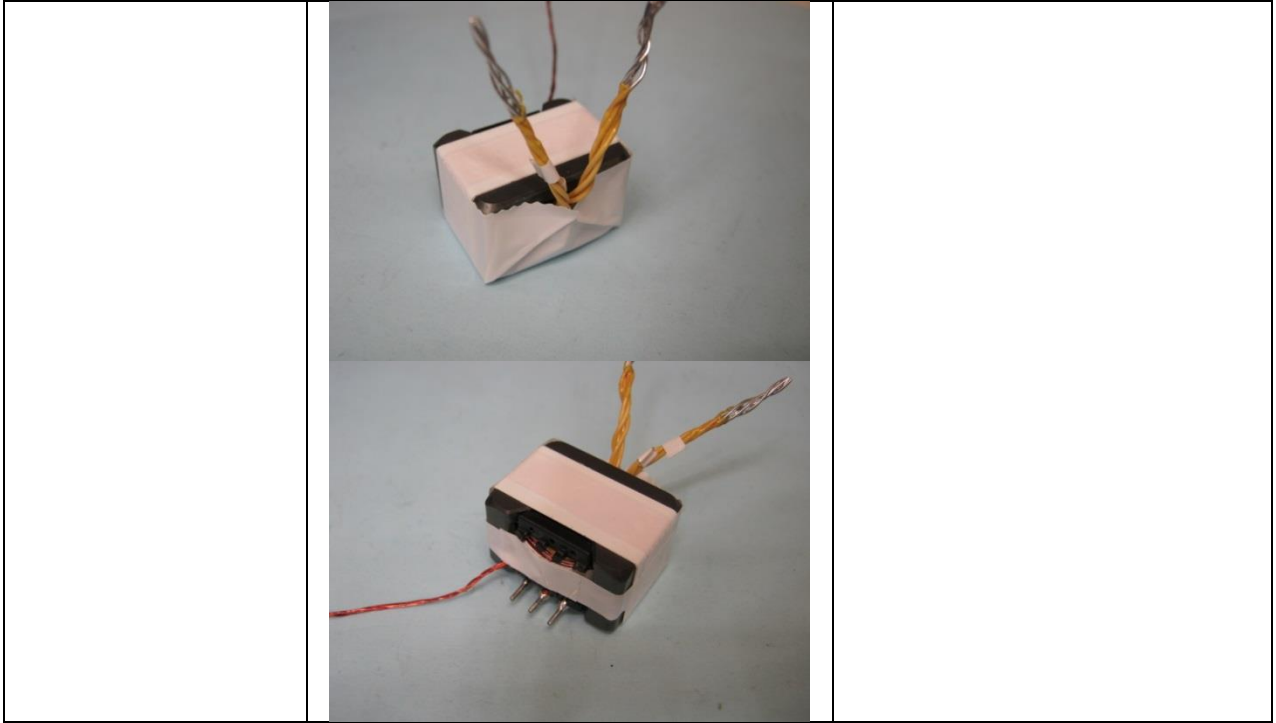
<p>Insulation</p>		<p>1 layer of tape Item [6].</p>
<p>WD5: Shield2</p>		<p>Start as FL3, wind 12 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.</p>

<p>Insulation</p>		<p>1 layer of tape Item [6].</p>
<p>WD6: 2nd Primary</p>		<p>Use floating wire from WD1-1st Primary, wind 14 turns from right to left. At the last turn, bring the wire back to left, and finish at pin 2.</p>

Finish



Place 1 layer of tape Item [6], bring the wires FL1 from secondary winding to the right at top slot of secondary-side of bobbin, and continue place 2 layers of tape.
 Gap cores to get 425 uH and secure with tape.
 Make flux band by using copper tape Item [8] which solder joint is off center and solder with wire Item [3] connect with FL3.
 Place 1 layer of tape to cover flux band.
 Varnish with Item [9].
 Place 2 layers of tape Item [7] at bottom core of transformer and wrap up to body of transformer then wrap 1 turn of tape Item [7] around the body of transformer, (see illustration beside).



8 Common Mode Choke Specifications

8.1 630 μH Common Mode Choke (L1)

8.1.1 Electrical Diagram

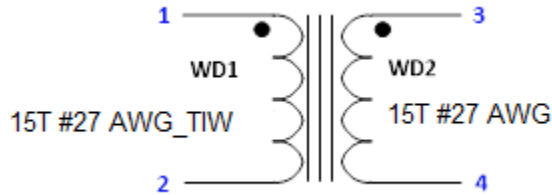


Figure 17 – Choke Electrical Diagram.

8.1.2 Electrical Specifications

Winding Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	630 μH ± 20%
---------------------------	---	--------------

8.1.3 Material List

Item	Description
[1]	Toroidal Core: 35T0375-10H, PI#: 32-00275-00.
[2]	Triple Insulated Wire: #27 AWG, Triple Coated.
[3]	Magnet Wire: #27 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

8.1.4 Common Mode Choke Construction

- Mark the start end of the winding as 1 and wind 15 turns of Item [2] on Item [1]. Mark the end of this winding as 2 for WD1.
- Repeat the same winding using Item [3], also wind 15 turns and interleave with WD1, mark start end as 3 and end as 4.
- Varnish using Item [4].



Figure 18 – 630 μ H CMC Illustration Image.

9 Transformer Design Spreadsheet

Power Supply Input			
Var	Value	Units	Description
VACMIN	90	V	Minimum Input AC Voltage (Manual Overwrite)
VACNOM	115	V	Nominal AC Voltage (For universal designs low line nominal voltage is displayed)
VACMAX	265	V	Maximum Input AC Voltage (Manual Overwrite)
FL	50	Hz	Line Frequency (Manual Overwrite)
TC	2.64	ms	Input Rectifier Conduction Time
VMIN	68.9	V	Minimum DC Input Voltage
VMAX	374.8	V	Maximum DC Input Voltage
ENCLOSURE	Adapter		Enclosure
TAMB	40	°C	Maximum Operating Ambient air Temperature (Manual Overwrite)
CIN	56.00	µF	Input Capacitance
Output Section			
Var	Value	Units	Description
PDP	45.00	W	Name Plate Power Rating
SET-POINT 1			
VO	20.00	V	Output Voltage
IO	2.25	A	Output Current
PO	45.00	W	Output Power
N	92.0	%	Converter efficiency for set-point (Manual Overwrite)
Z	0.57		Loss Allocation Factor for set-point
SET-POINT 2			
VO	15.00	V	Output Voltage
IO	3.00	A	Output Current
PO	45.00	W	Output Power
N	92.0	%	Converter efficiency for set-point (Manual Overwrite)
Z	0.57		Loss Allocation Factor for set-point
SET-POINT 3			
VO	9.00	V	Output Voltage
IO	3.00	A	Output Current
PO	27.00	W	Output Power
N	92.0	%	Converter efficiency for set-point (Manual Overwrite)
Z	0.56		Loss Allocation Factor for set-point
SET-POINT 4			
VO	5.00	V	Output Voltage
IO	3.00	A	Output Current
PO	15.00	W	Output Power
N	91.0	%	Converter efficiency for set-point (Manual Overwrite)
Z	0.54		Loss Allocation Factor for set-point
Device Variables			
Var	Value	Units	Description
Device	INN3379C		PI Device Name
Current Limit Mode	Increased		Device Current Limit Mode
BVDSS	750	V	Drn-Src Bkdn Voltage
ILIMITMIN	1.980	A	Minimum Current Limit
ILIMITTYP	2.130	A	Typical Current Limit
ILIMITMAX	2.279	A	Maximum Current Limit
RDSON	0.49	Ω	PI Device RDSON (100°C)
RDSON_25C	0.30	Ω	PI Device RDSON (25°C)
UVOV_PRIORITY	Overvoltage		Input Undervoltage/Overvoltage Priority type
RTH_DEVICE	167.84	°C/W	PI Device Heatsink Maximum Thermal Resistance
DEV_HSINK_TYPE	2 Oz (70 µ) 2-Sided Copper PCB		PI Device Heatsink Type
DEV_HSINK_AREA	104	mm ²	PI Device Heatsink Area
Clamp Circuit			
Var	Value	Units	Description



Clamp Type	RCD Clamp		Clamp Circuit Type
VCLAMP_ESTIMATED	273.62	V	Estimated Clamping Voltage above VMAX
VDRAIN Estimated	648.39	V	Estimated Drain Voltage
Electrical Parameters (Worst case)			
Var	Value	Units	Description
VDS	0.34	V	On state Drain to Source Voltage
FS	70000	Hz	Switching Frequency (at VMIN and Full Load) (Manual Overwrite)
KP	0.772		Continuous/Discontinuous Operating Ratio (at VMIN and Full Load)
VOR	140.00	V	Reflected Output Voltage (Manual Overwrite)
DMAX	0.669		Maximum Duty Cycle (at VMIN and Full Load)
TIME_ON	13.13	µs	Primary controller on-time. See Information section for detail
TIME_OFF	4.90	µs	Expected Device Off-time (at VMIN and Full Load)
IP	2.102	A	Peak Primary Current (at VMIN and Full Load)
IAVG	0.70	A	Primary Average Current (at VMIN and Full Load)
IRMS	0.994	A	Primary RMS Current (at VMIN and Full Load)
IR	2.097	A	Primary Ripple Current (at VMIN and Full Load)
ISP	14.712	A	Peak Secondary Current
ISRMS	5.620	A	Secondary RMS Current
IRIPPLE	4.752	A	Output Capacitor - RMS Ripple Current
Primary Bias Variables			
Var	Value	Units	Description
VB	7.5	V	Bias Voltage (Manual Overwrite)
VBMIN	12.2	V	Minimum Bias Voltage
VBMAX	53.2	V	Maximum Bias Voltage
BIAS_REG_TYPE	Linear Regulator		Bias Circuit Type
PIVB	147	V	Bias Rectifier Maximum Peak Inverse Voltage
NB	7		Primary Bias Winding Number of Turns
Transformer Construction Parameters			
Var	Value	Units	Description
Core Type	ATQ23.714		Core Type (Manual Overwrite)
Core Material	3F3		Core Material
Bobbin Reference	Generic, 4 pri. + 4 sec.		Bobbin Reference
Bobbin Orientation	Horizontal		Bobbin type
Primary Pins	4		Number of Primary pins used
Secondary Pins	2		Number of Secondary pins used
USE_SHIELDS	YES		Use shield Windings
LPmin	400.00	µH	Minimum Primary Inductance
LP_nom	418	µH	Nominal Primary Inductance
LP_MAX	439.40	µH	Maximum Primary Inductance
LP_Tol	5.0	%	Primary Inductance Tolerance
NP	28.0		Calculated Primary Winding Total Number of Turns
NSM	4		Secondary Main Number of Turns
CMA	258	Cmils/A	Primary Winding Current Capacity
BW	6.60	mm	Bobbin Winding Width
ML	0.00	mm	Safety Margin on Left Width
MR	0.00	mm	Safety Margin on Right Width
FF	115.97	%	Actual Transformer Fit Factor.
AE	103.00	mm ²	Core Cross Sectional Area
ALG	534	nH/T ²	Gapped Core Specific Inductance
BM	3159	Gauss	Maximum Flux Density
BP	3554	Gauss	Peak Flux Density
BAC	1579	Gauss	AC Flux Density for Core Loss
LG	0.219	mm	Estimated Gap Length
L_LKG	4.20	µH	Estimated primary leakage inductance (Manual Overwrite)
LSEC	20	nH	Secondary Trace Inductance
Primary Winding Section 1			
Var	Value	Units	Description

NP1	14		Number of Primary Winding Turns in the First Section of Primary
Wire Size	26	AWG	Primary Winding - Wire Size (Manual Overwrite)
Winding Type	Single (x1)		Primary Winding - Number of Parallel Wire Strands (Manual Overwrite)
L	0.96		Primary Winding - Number of Layers
Primary Winding Section 2			
Var	Value	Units	Description
NP2	14		Rounded (Integer) Number of Primary winding turns in the second section of primary
Wire Size	26	AWG	Primary Winding - Wire Size (Manual Overwrite)
Winding Type	Single (x1)		Primary Winding - Number of Parallel Wire Strands (Manual Overwrite)
L2	0.96		Primary Number of Layers in 2nd split winding
Output 1			
Var	Value	Units	Description
Cable Drop Compensation	0	%	Cable Drop Compensation
NS	4		Secondary Number of Turns
Wire Size	24	AWG	Wire size of secondary winding (Manual Overwrite)
Winding Type	Quadfilar (x4)		Output winding number of parallel strands (Manual Overwrite)
L_S_OUT	1.82		Secondary Output Winding Layers
PIVS	73.54	V	Output Rectifier Maximum Peak Inverse Voltage
ISP	14.712	A	Peak Secondary Current
ISRMS	5.620	A	Secondary RMS Current
RTH_RECTIFIER	31.60	°C/W	Output Rectifier Heatsink Maximum Thermal Resistance
OR_HSINK_TYPE	Custom Aluminum		Output Rectifier Heatsink Type
OR_HSINK_AREA	1193	mm ²	Output Rectifier Heatsink Area
OSR_RDSON	42.00	mΩ	Synchronous Rectifier RDSON
CO	330 x 2	μF	Output Capacitor - Capacitance
IRIPPLE	4.752	A	Output Capacitor - RMS Ripple Current
Expected Lifetime	136819	hr	Output Capacitor - Expected Lifetime

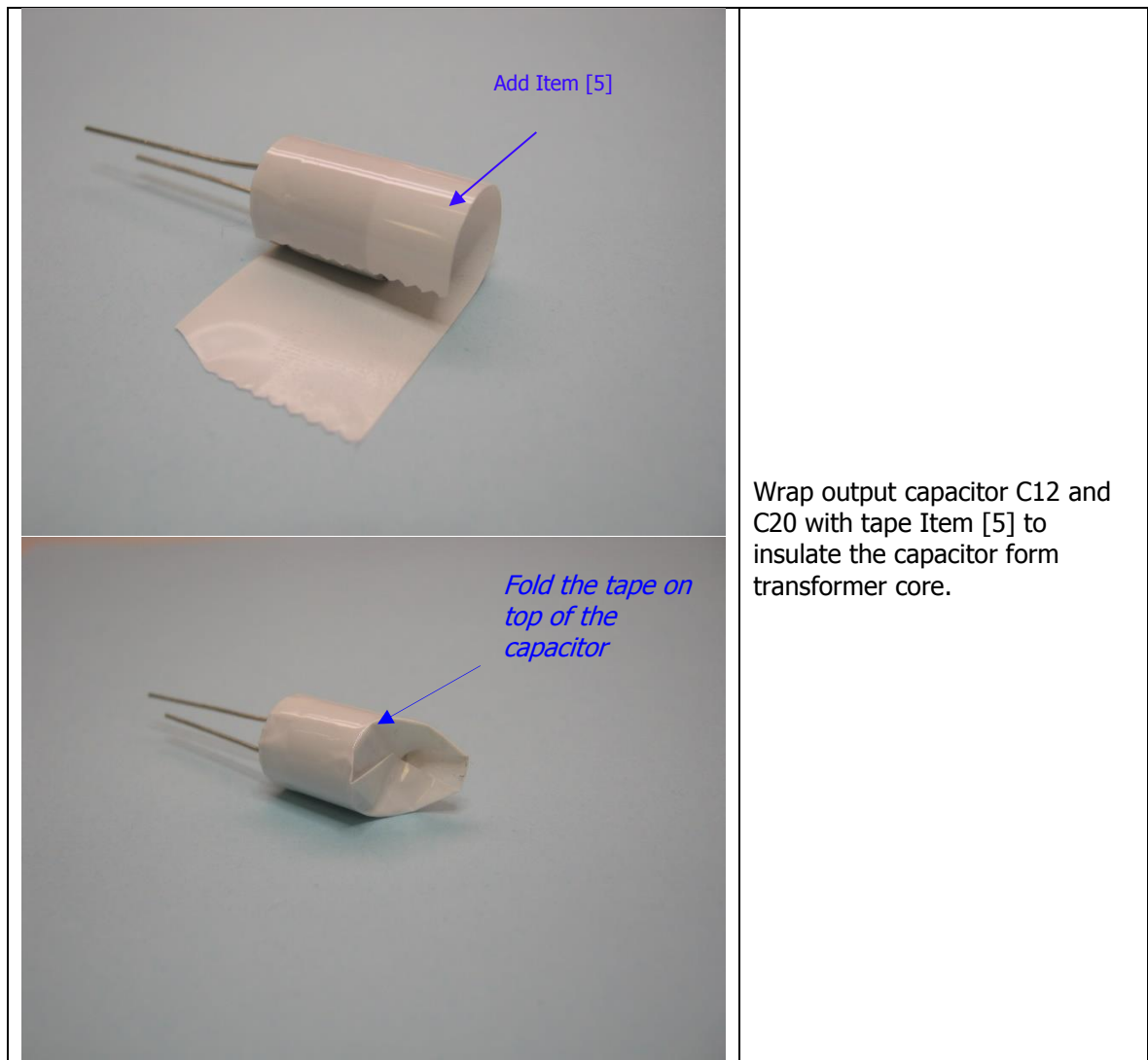
10 PCB Assembly Instructions

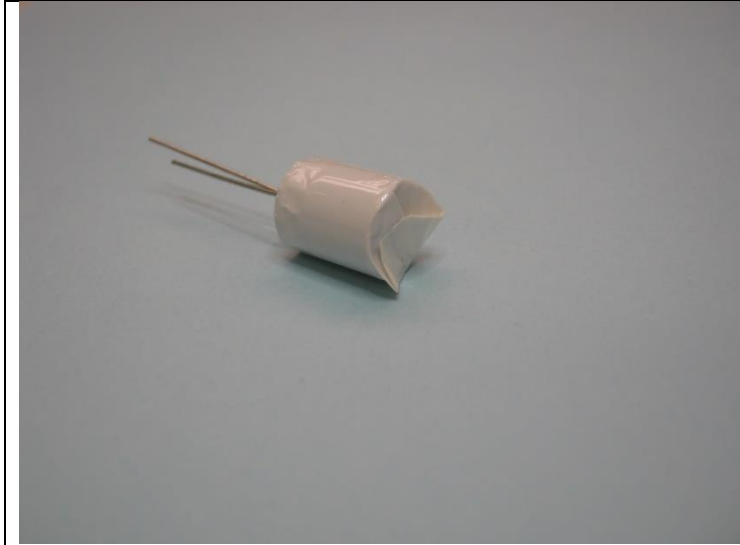
10.1 Material List

Item	Description
[1]	Output Capacitor C12 &C20 on DER-600 Schematic.
[2]	Bulk Capacitor C2 on DER-600 Schematic.
[3]	Bias Capacitor C5 on DER-600 Schematic.
[4]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 16.4 mm Wide, 13 mm Long.
[5]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 18.2 mm Wide, 30 mm Long.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 36 mm Wide, 50 mm Long.
[7]	Teflon Tubing #22.

10.2 Capacitors Assembly Taping Instructions

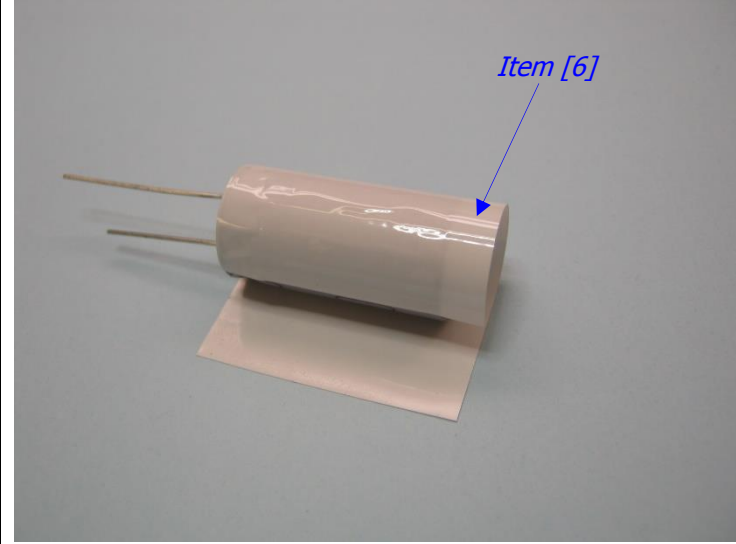
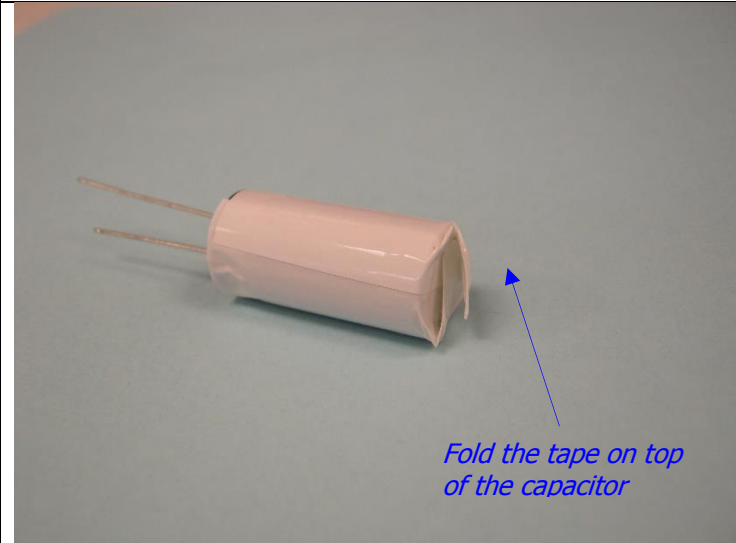
10.2.1 Output Capacitor C12 and C20 Taping Instructions



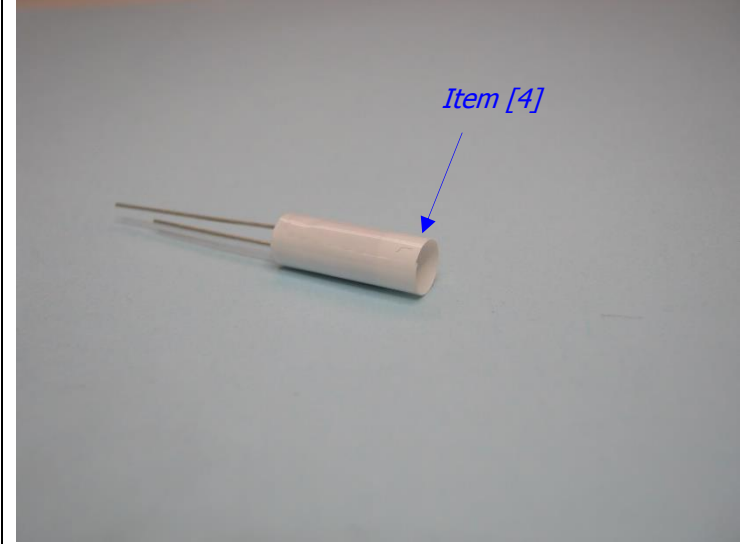
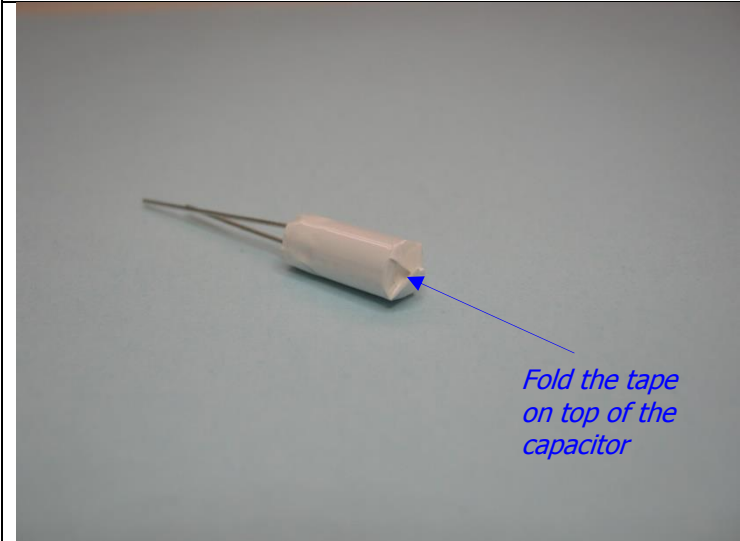


Completed C12 capacitor.

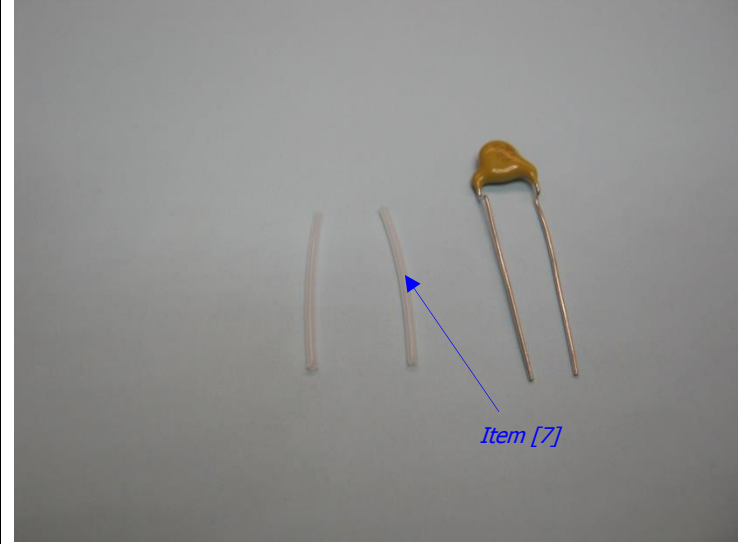

10.2.2 Bulk Capacitor C2 Taping Instructions

 <p><i>Item [6]</i></p>	<p>Wrap bulk capacitor C2 with tape Item [6] to insulate the capacitor from transformer core</p>
 <p><i>Fold the tape on top of the capacitor</i></p>	<p>Completed tape C2 capacitor.</p>

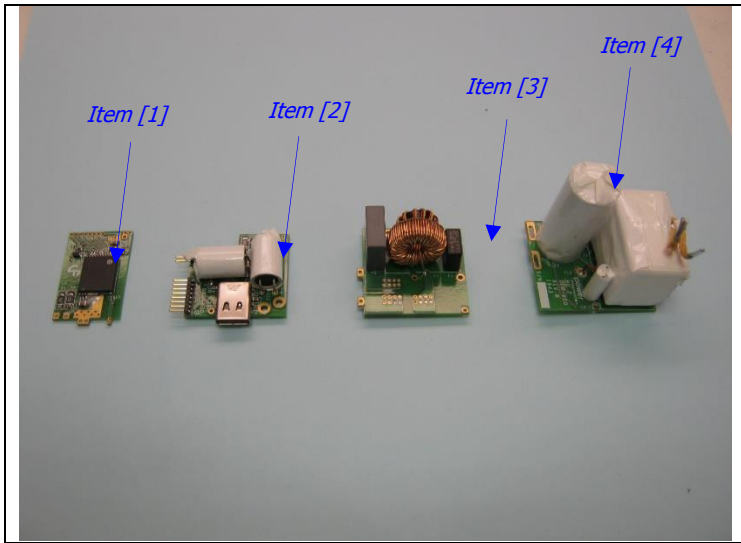
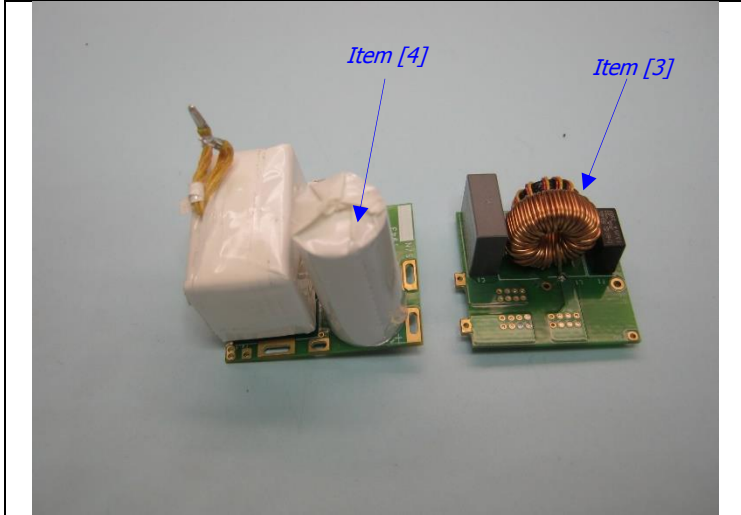
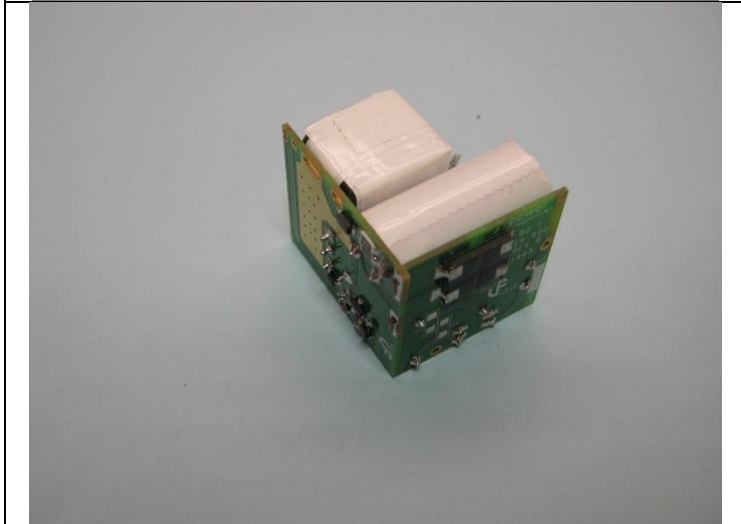
10.2.3 Bias Capacitor Taping Instructions

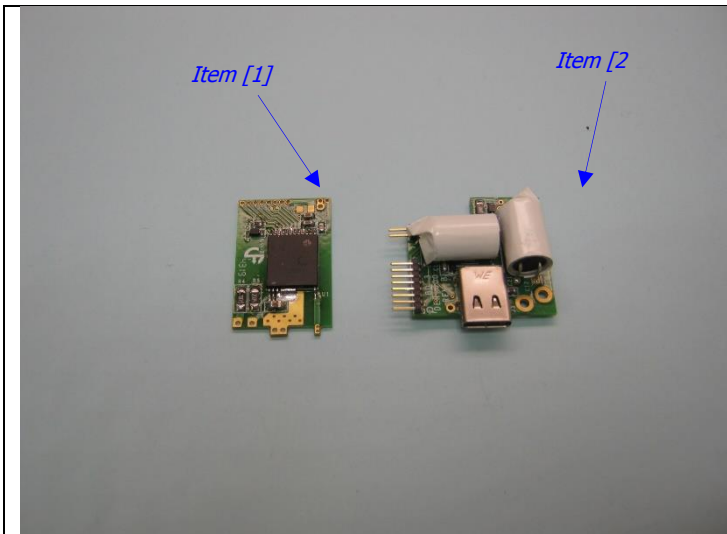
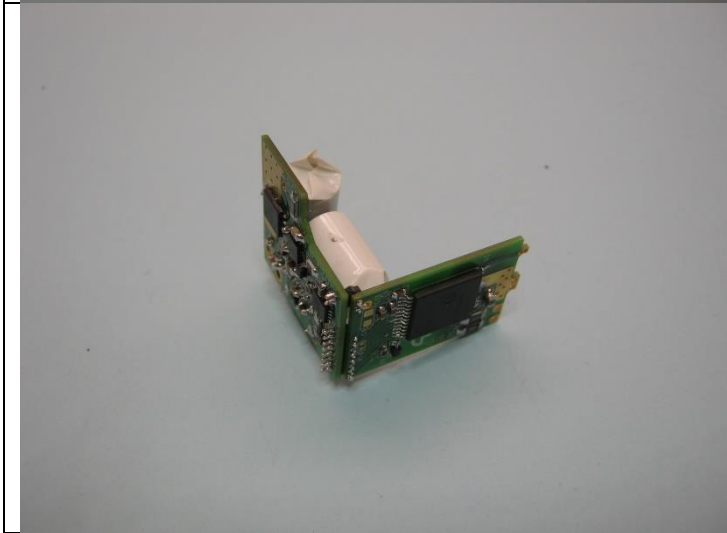
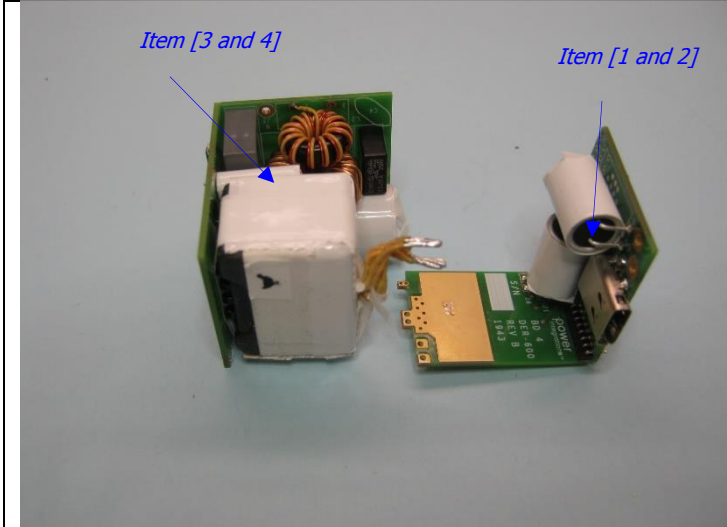
 <p><i>Item [4]</i></p>	<p>Wrap bias capacitor C5 with tape Item [4] to insulate the capacitor from transformer core.</p>
 <p><i>Fold the tape on top of the capacitor</i></p>	<p>Completed tape C5 capacitor.</p>

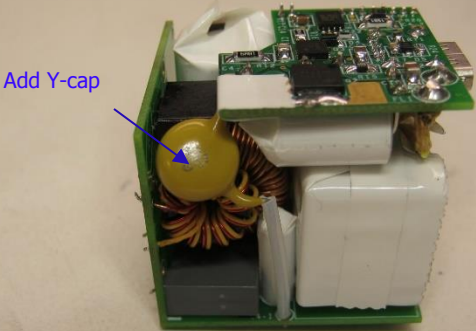

10.2.4 Y Capacitor Sleeving Instructions

	<p>Cut 2 pcs Item [7] 24 mm long.</p>
	<p>Insert Item [7] into Y capacitor.</p>

10.3 Daughter Boards Assembly Instructions

	<p>Assembled daughter boards</p> <ul style="list-style-type: none">[1] – InnoSwitch-pro board[2]- USB Type-C board[3] Input EMI board[4] Main board
	<p>Solder Item [3] and [4] together</p>
	<p>Item [3] and [4] – after soldering</p>

	<p>Solder Item [1] and [2] together</p>
	<p>Item [1] and [2] together – after soldering</p>
	<p>Solder Item [1&2] and [3&4] boards together.</p>

	<p>Assybled Item [1&2] and [3&4] boards.</p>
	<p>Add y-cap connecting Item [1] and Item [4]</p>
	<p>Finished unit.</p>

11 Adapter Case and Thermal Pad Assembly

11.1 Material List

Item	Description
[1]	Thermal pad #1, use 3M ,0.02" Thickness , PI#: 66-00075-00 Cut into Dimension: 0.5"x 0.2".
[2]	Thermal pad #1, use 3M ,0.02" Thickness , PI#: 66-00075-00 Cut into Dimension: 0.95"x 0.68".
[3]	Enclosure: body material: ABS Filament, size: 1.75 mm.

11.2 Adapter Case Dimensions

Note: Dimensions are in millimeters.

11.2.1 Case Body

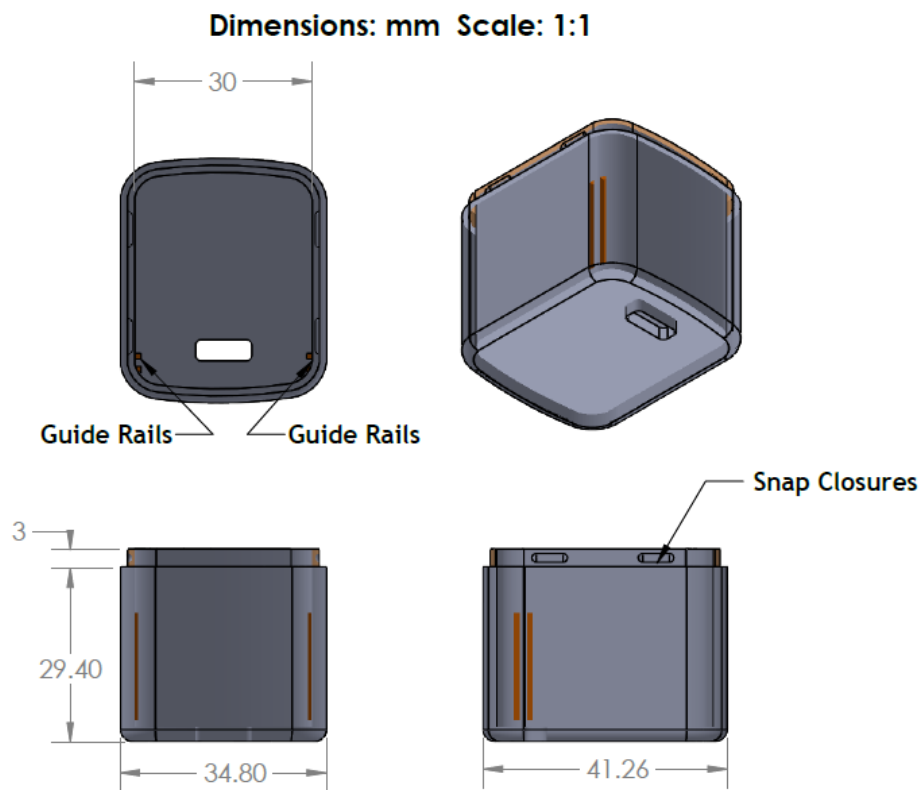


Figure 19 – Adapter Case Body Dimensions.

11.2.2 Case Cap

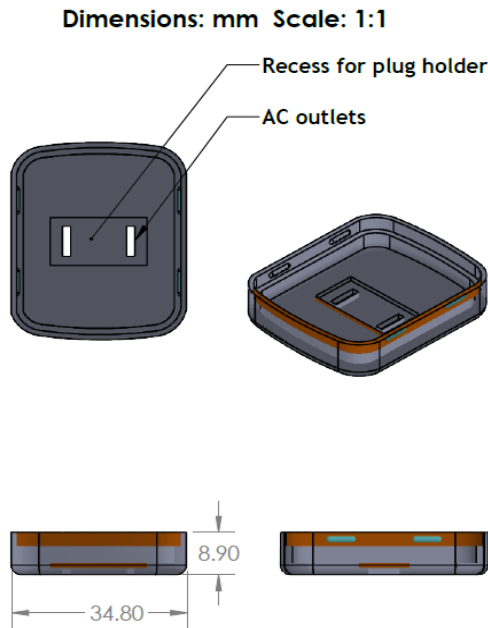


Figure 20 – Adapter Case Cap Dimensions.

11.3 Thermal Pad Dimensions

Thermal pad dimensions for the Innoswitch board are as given below.

11.3.1 Thermal Pad

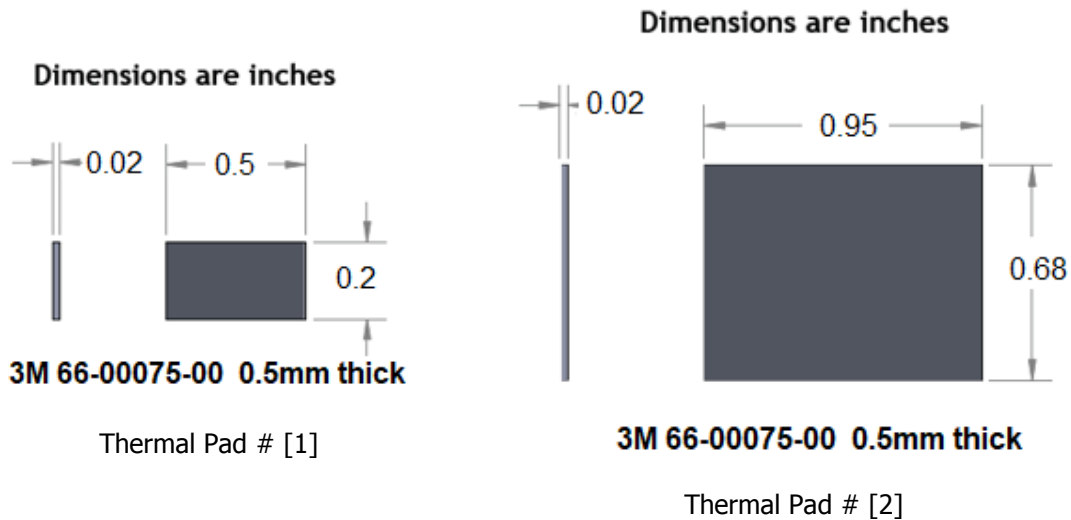

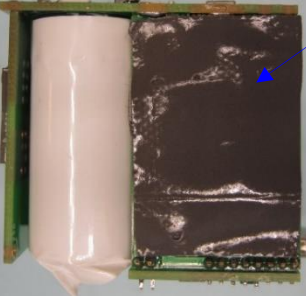

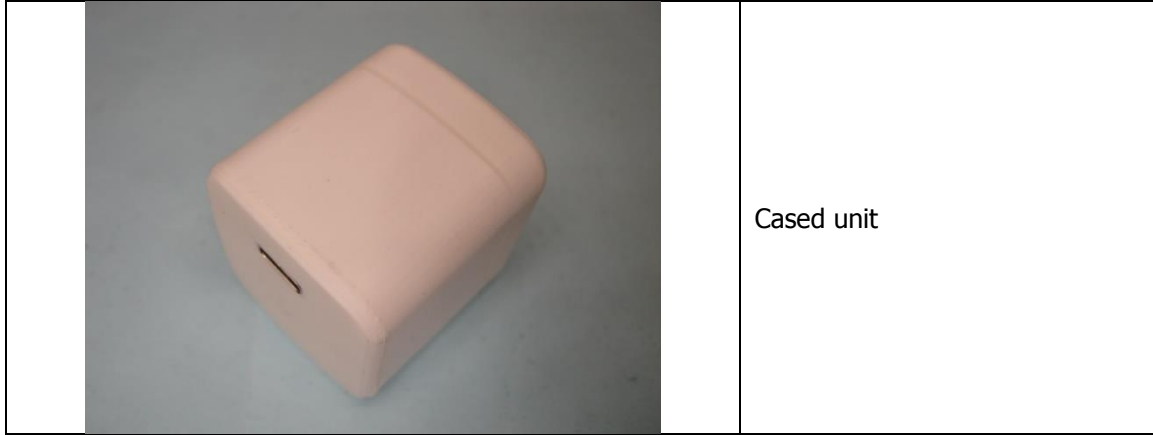


Figure 21 – Thermal Pad Dimensions.

11.4 Thermal Pad and Case Assembly Illustrations

	 <p data-bbox="686 300 889 327">Add Thermal pad # 1</p>		<p data-bbox="1027 474 1263 506">Add thermal Pad #1</p>
	 <p data-bbox="773 751 894 779">Add Thermal pad # 2</p>		<p data-bbox="1027 905 1263 936">Add thermal Pad #2</p>
			<p data-bbox="1027 1318 1398 1381">Inserting the assembly into the case</p>



12 Performance Data

Note 1: Output voltages measured on the PCB end
2: Measurements taken at room temperature (approximately 24 °C)

12.1 No-Load Input Power at 5 V_{OUT}

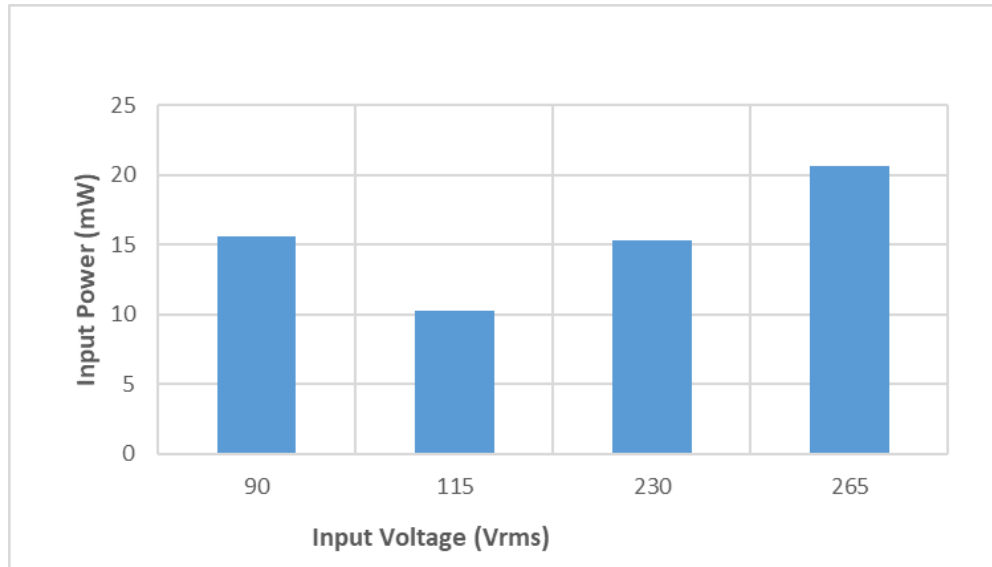


Figure 22 – No-Load Input Power vs. Input Line Voltage.

12.2 Average and 10% Load Efficiency

Note: Output voltage measured at the USB-PD connector on the board. Efficiency measured at room temperature after warming up the unit for 30min @ full load.

12.2.1 Efficiency Requirements

V _{OUT} (V)	Model (V)	Power (W)	Test	Average	Average	10% Load
			Effective	2016	Jan-16	Jan-16
			New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2	
5	<6	15	81.4%	81.8%	72.5%	
9	>6	27	86.6%	87.3%	77.3%	
15	>6	45	88.0%	88.9%	78.9%	
20	>6	45	88.0%	89.0%	79.0%	

12.2.2 Efficiency Performance Summary (On Board)

V _{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	15	91.37	89.69	87.56	83.42
9	27	92.24	91.41	87.82	84.54
15	45	92.54	92.23	87.70	85.19
20	45	92.08	91.81	85.43	82.98

12.2.3 Average and 10% Load Efficiency at 115 VAC

12.2.3.1 Output: 5 V / 3 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.05	91.61	91.37
75	11.32	91.73	
50	7.57	91.63	
25	3.79	90.51	
10	1.52	87.56	

12.2.3.2 Output: 9 V / 3 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.00	92.64	92.24
75	20.29	92.54	
50	13.56	92.50	
25	6.78	91.30	
10	2.72	87.82	

12.2.3.3 Output: 15 V / 3 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	44.91	93.01	92.54
75	33.76	92.96	
50	22.55	92.65	
25	11.28	91.53	
10	4.51	87.70	

12.2.3.4 Output: 20 V / 2.25 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	44.84	92.89	92.08
75	33.52	92.73	
50	22.46	92.17	
25	11.09	90.53	
10	4.50	85.43	

12.2.4 Average and 10% Load Efficiency at 230 VAC

12.2.4.1 Output: 5 V / 3 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	15.10	90.90	89.69
75	11.35	90.61	
50	7.58	89.86	
25	3.79	87.38	
10	1.52	83.43	

12.2.4.2 Output: 9 V / 3 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	27.05	92.44	91.41
75	20.33	92.21	
50	13.57	91.60	
25	6.79	89.41	
10	2.72	84.55	

12.2.4.3 Output: 15 V / 3 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	44.99	93.16	92.23
75	33.80	92.96	
50	22.56	92.37	
25	11.28	90.44	
10	4.51	85.19	

12.2.4.4 Output: 20 V / 2.25 A

Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%) [100% - 25% Load]
100	44.91	93.11	91.81
75	33.56	92.70	
50	22.48	92.00	
25	11.10	89.44	
10	4.50	82.97	

12.3 Efficiency Across Load (On Board)

12.3.1 Output: 5 V / 3 A

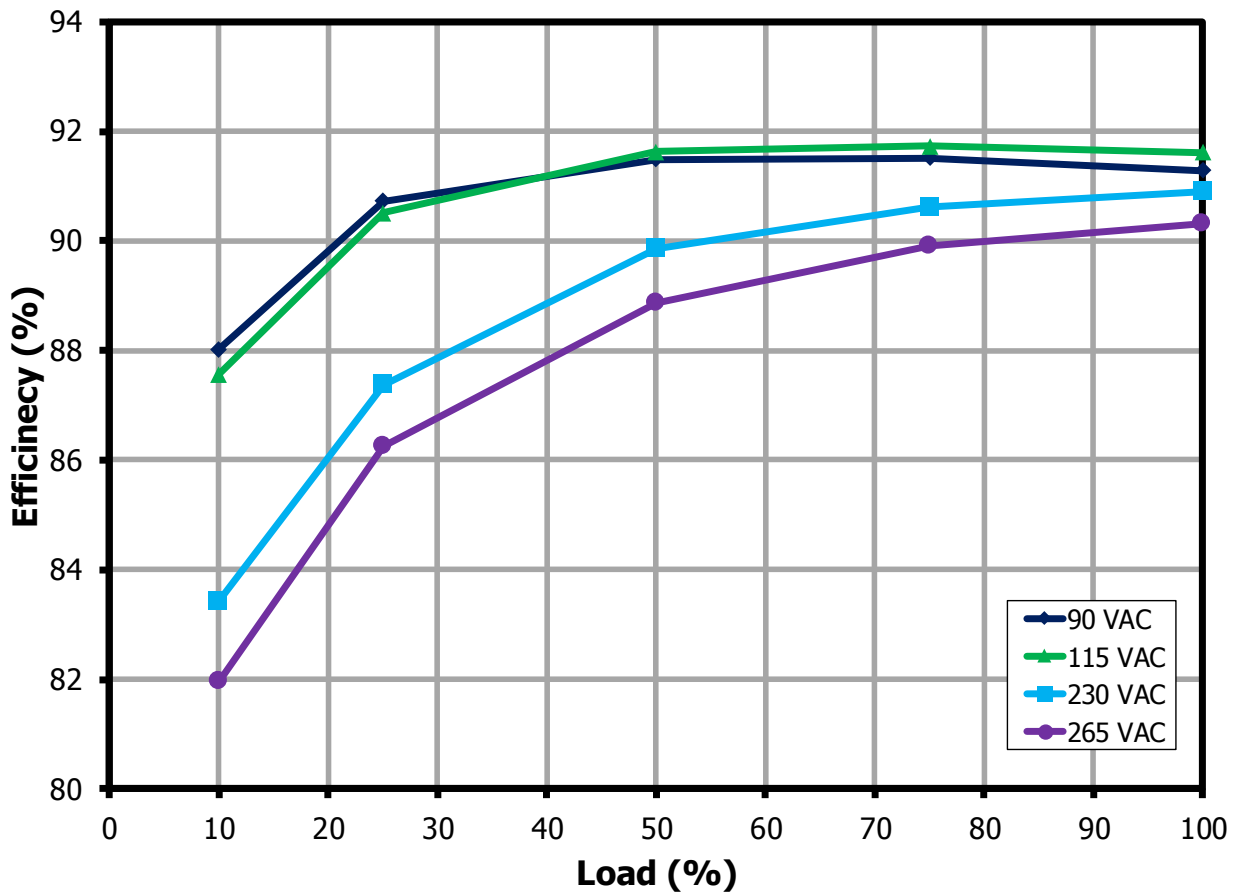


Figure 23 – Efficiency vs. Load for 5 V Output, Room Temperature.

12.3.2 Output: 9 V / 3 A

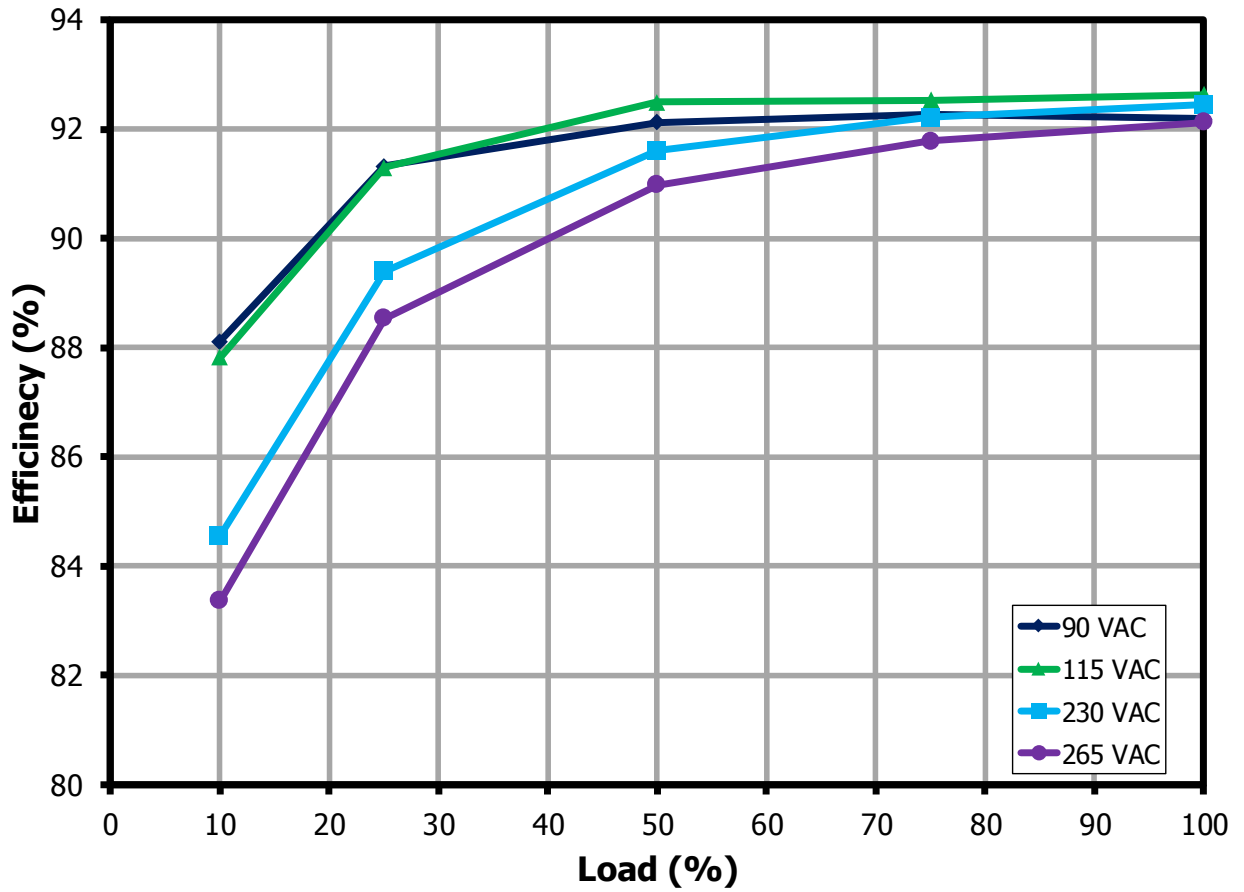


Figure 24 – Efficiency vs. Load for 9 V Output, Room Temperature.



12.3.3 Output: 15 V / 3 A

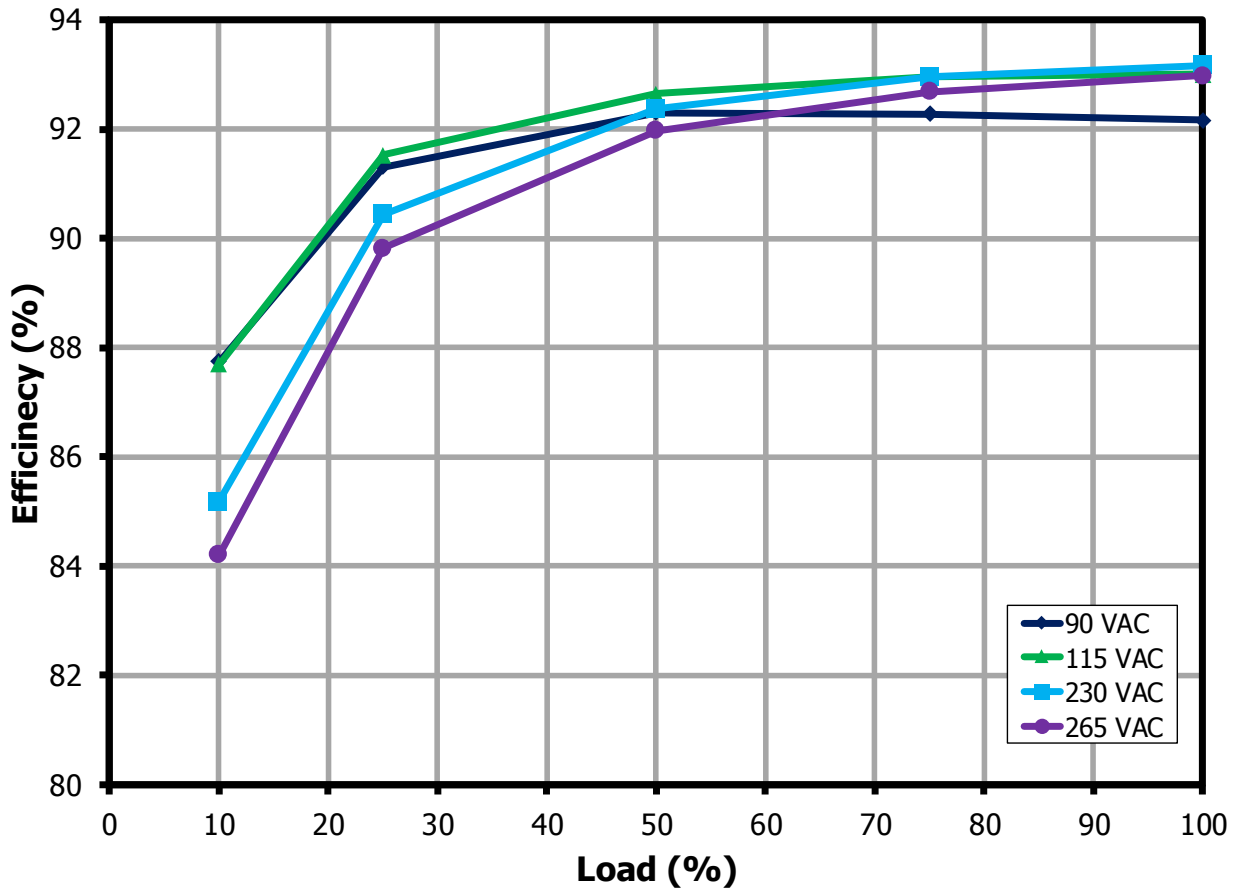


Figure 25 – Efficiency vs. Load for 15 V Output, Room Temperature.

12.3.4 Output: 20 V / 2.25 A

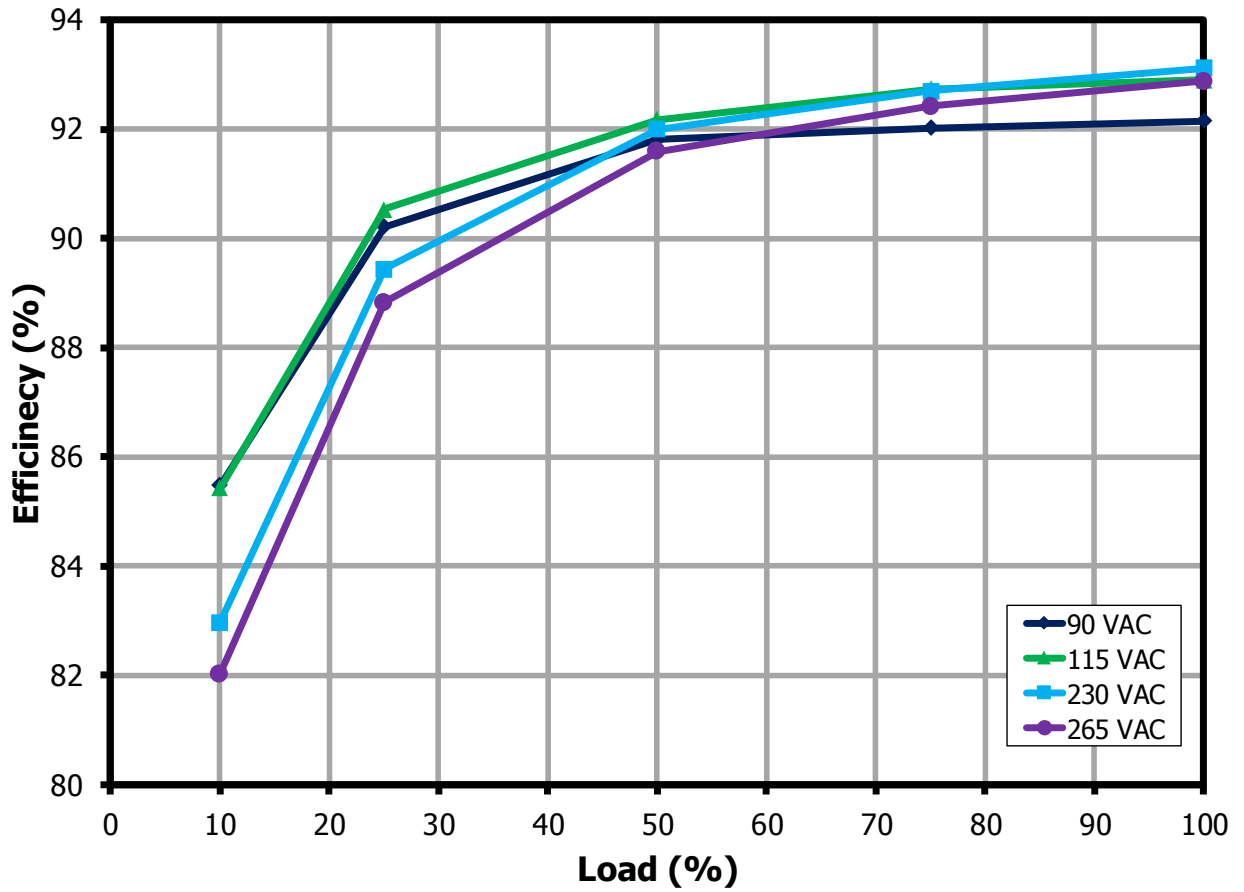


Figure 26 – Efficiency vs. Load for 20 V Output, Room Temperature.



12.4 Efficiency Across Line (On Board)

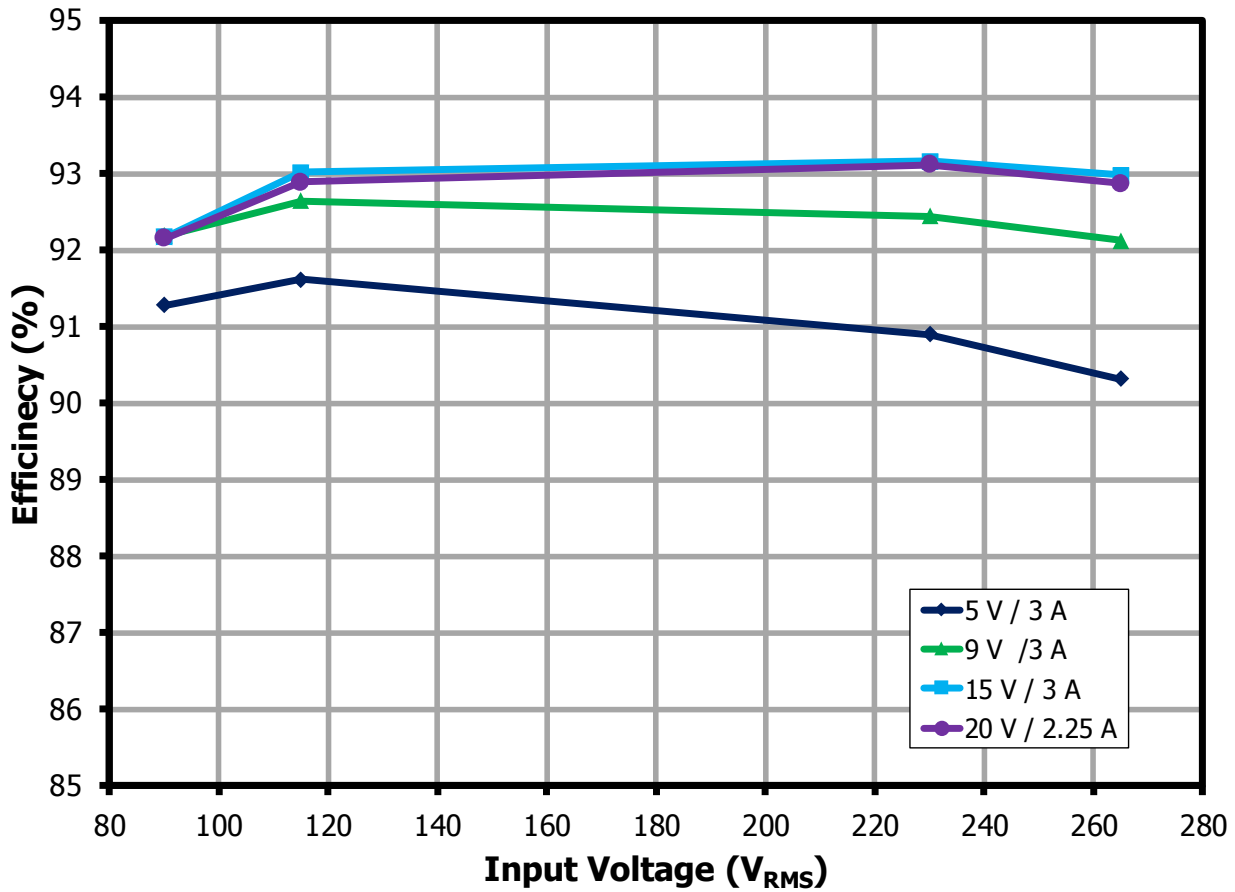


Figure 27 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 15 V, and 20 V Output, Room Temperature.

12.5 Load Regulation (On Board)

12.5.1 Output: 5 V / 3 A

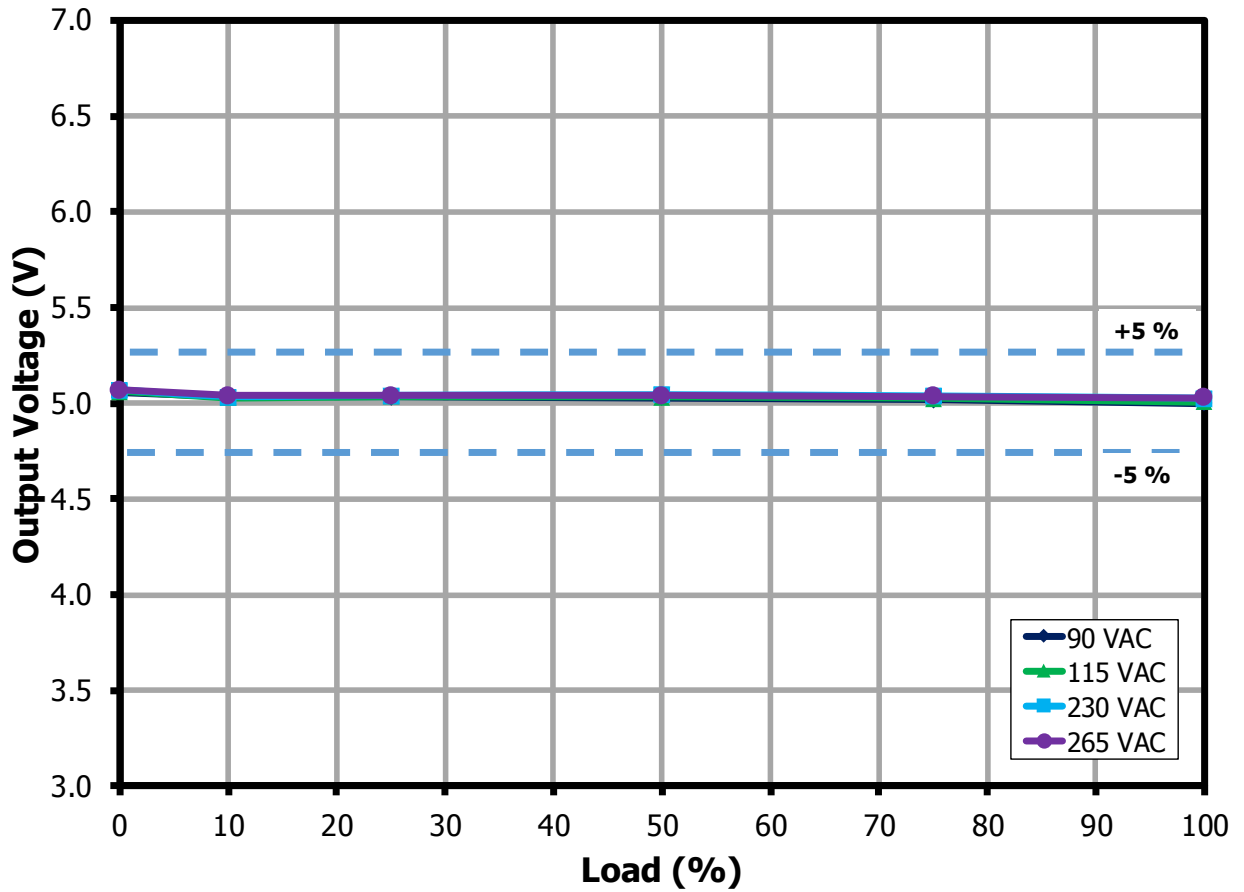


Figure 28 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.



12.5.2 Output: 9 V / 3 A

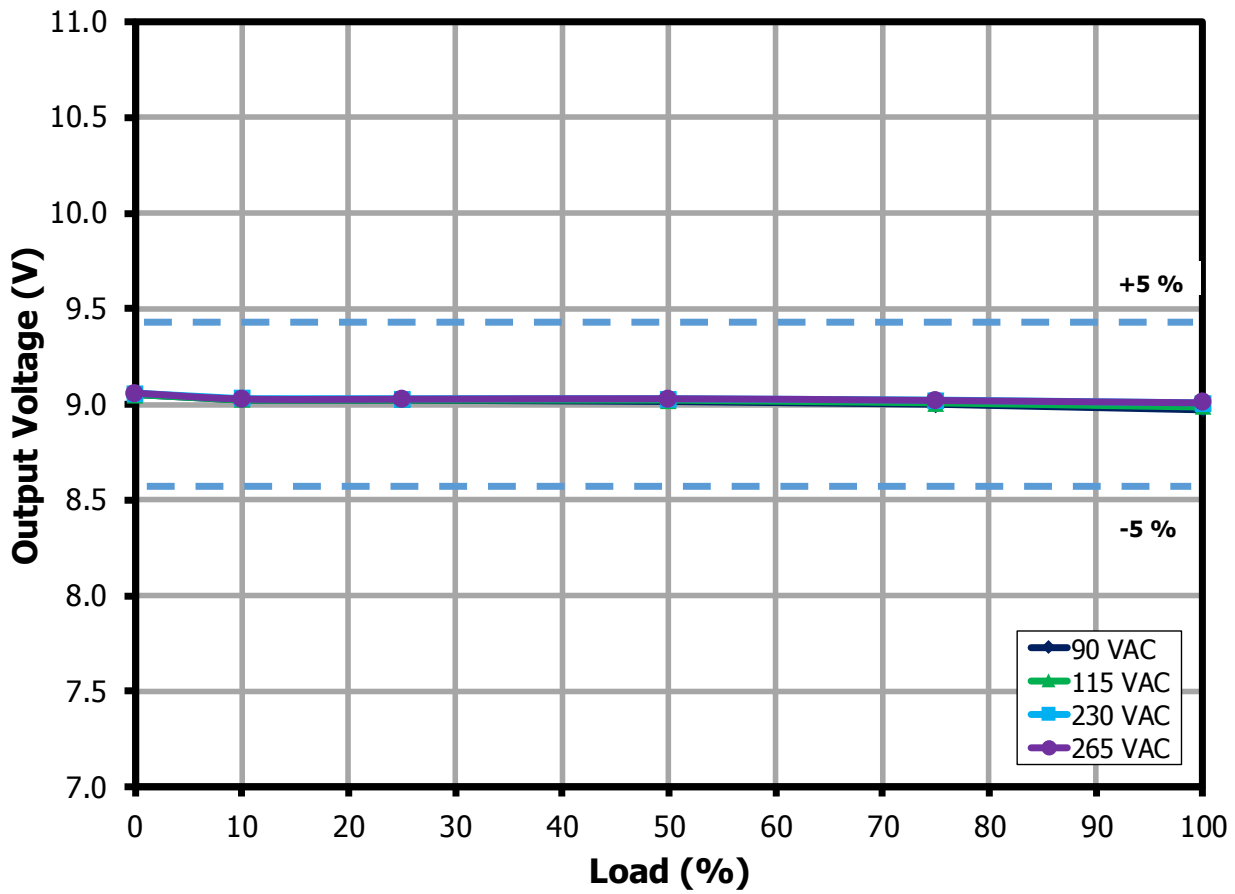


Figure 29 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

12.5.3 Output: 15 V / 3 A

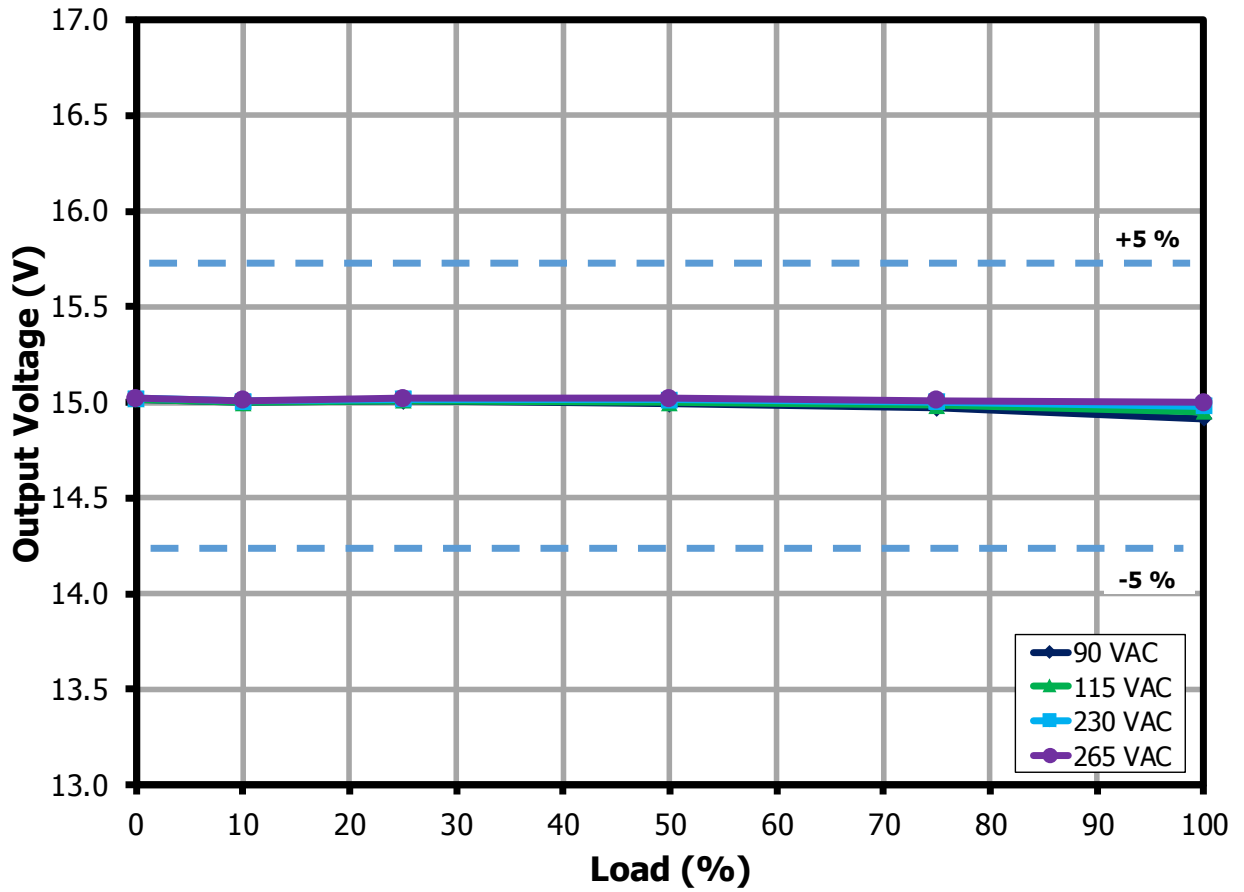


Figure 30 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.



12.5.4 Output: 20 V / 2.25 A

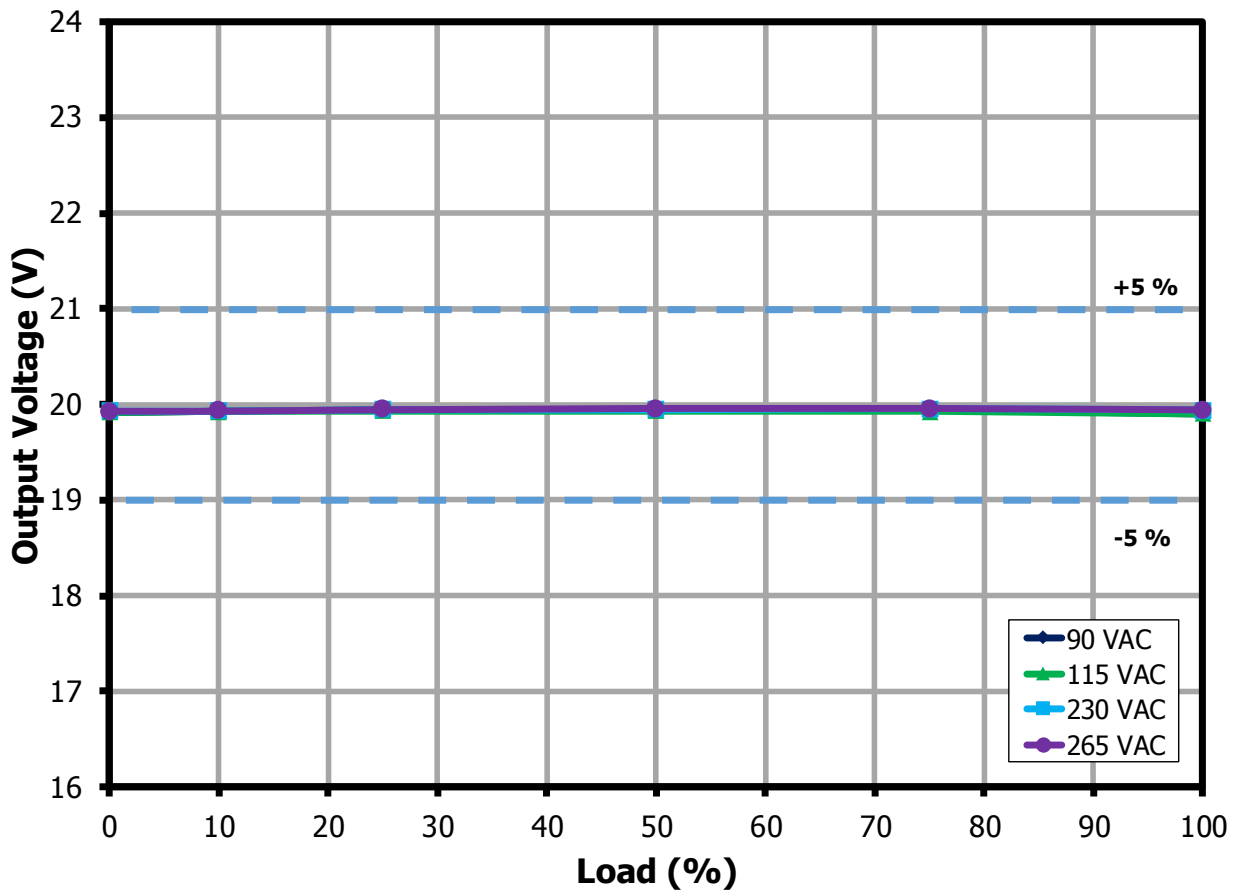


Figure 31 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

12.6 Line Regulation (On Board)

12.6.1 Output: 5 V / 3 A

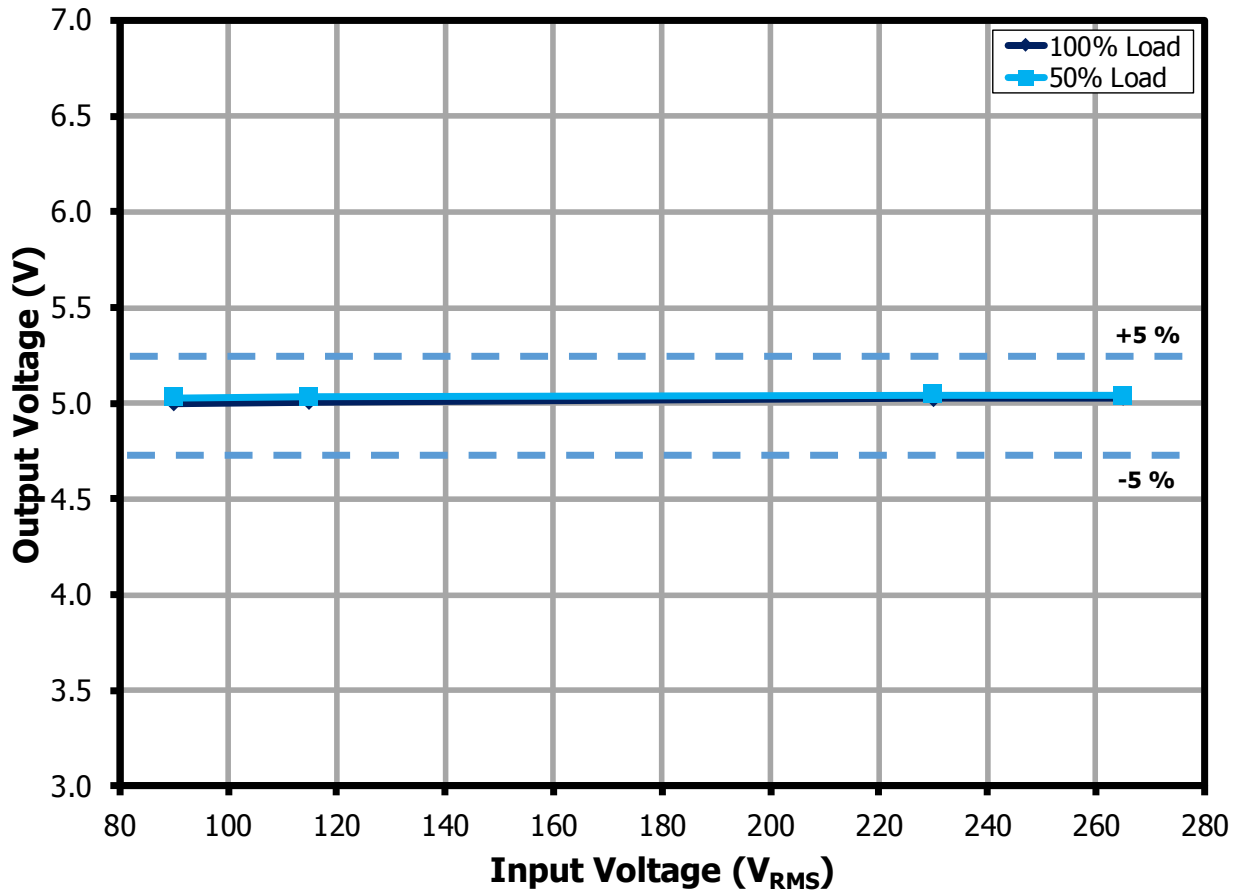


Figure 32 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.



12.6.2 Output: 9 V / 3 A

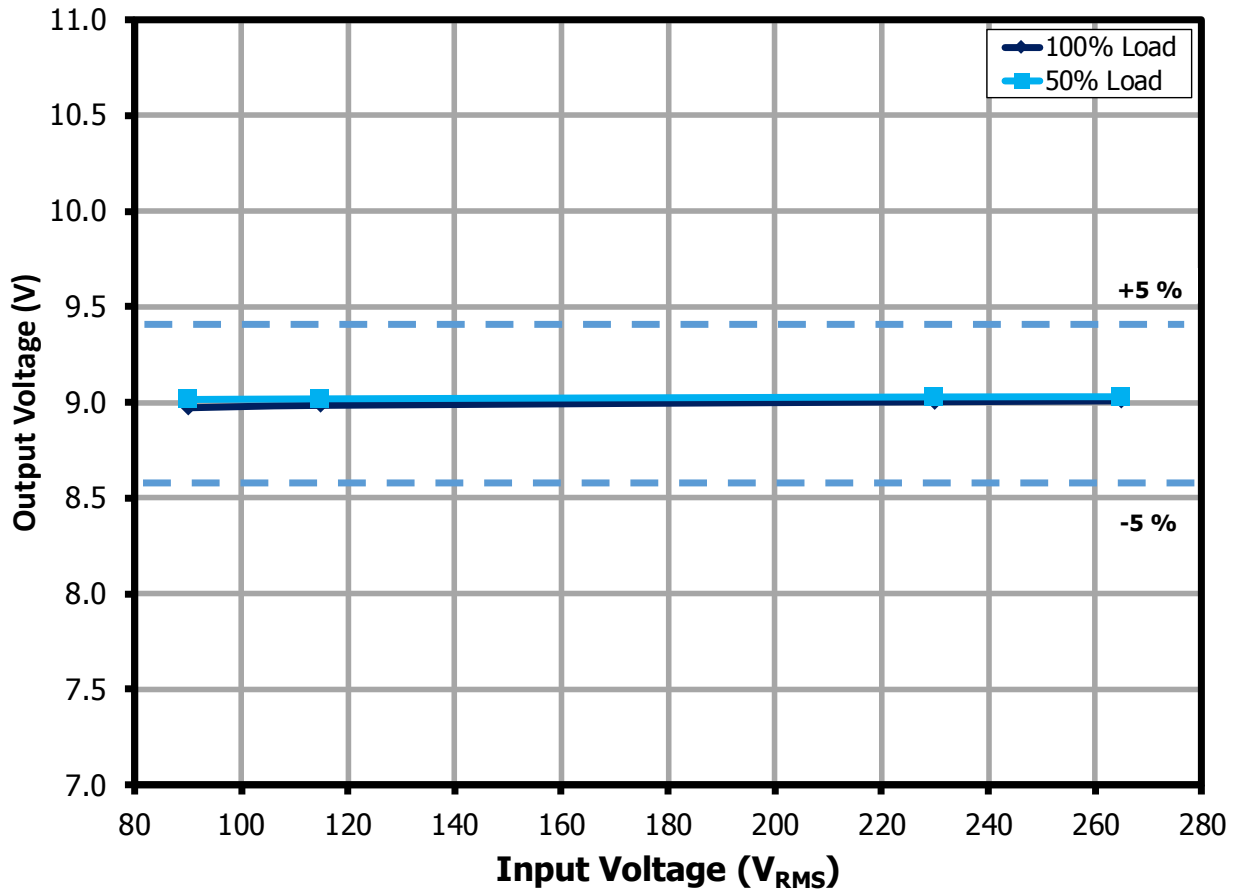


Figure 33 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

12.6.3 Output: 15 V / 3 A

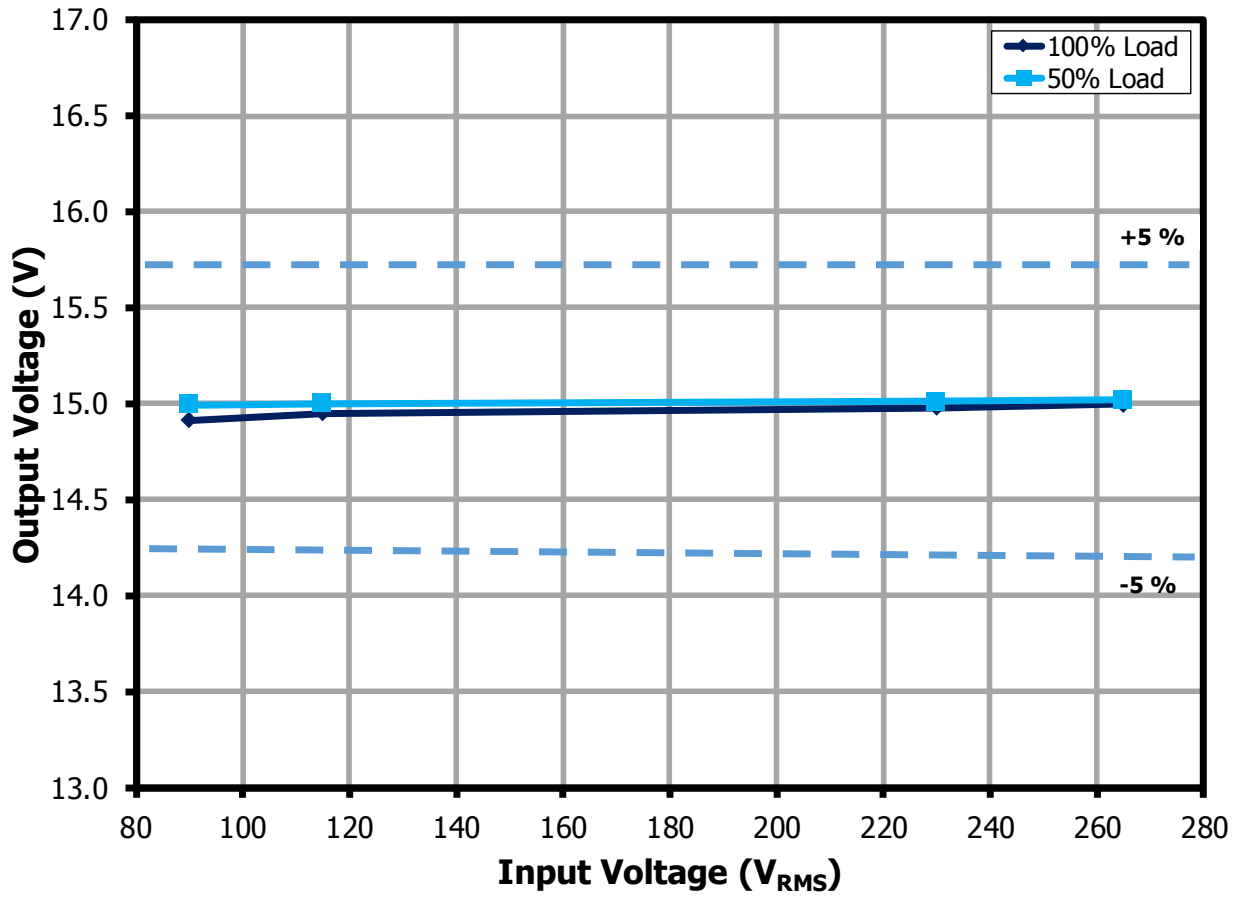


Figure 34 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.



12.6.4 Output: 20 V / 2.25 A

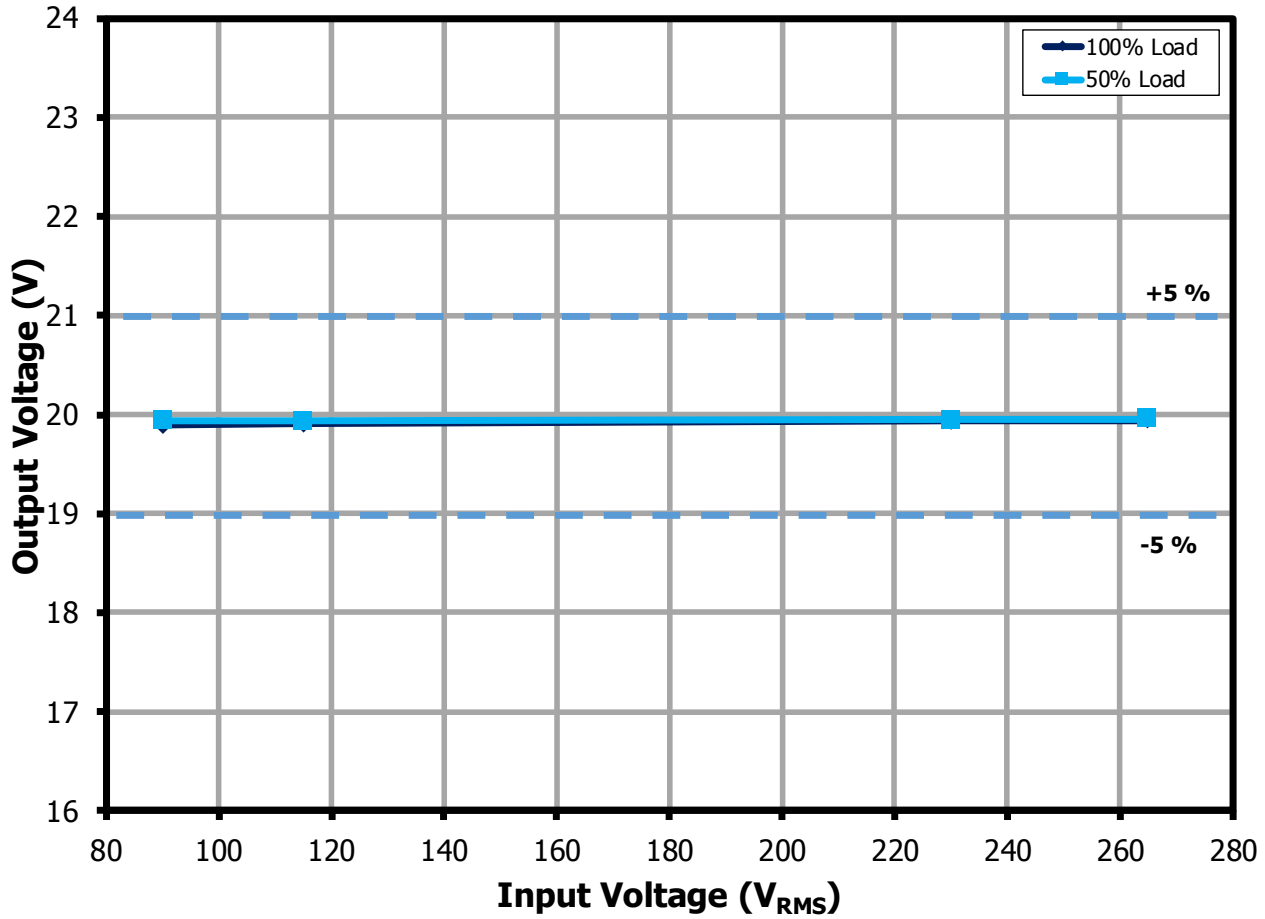


Figure 35 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

13 Thermal Performance

13.1 Thermal Performance with Adapter Case Enclosure

Note 1: Thermocouples are attached to monitor various devices temperatures.

13.1.1 Output: 20 V / 2.25 A (90 VAC /265 VAC), Ambient Temperature: 25 °C

Component	Temperature (°C)	
	20 V / 2.25 A @ 90 VAC	20 V / 2.25 A @ 265 VAC
Case	58.2	55.4
Bridge Rectifier, BR1	93.9	68.7
Bulk Capacitor, C2	84.3	69.7
Transformer, T1 - Core	85.3	83.0
Transformer, T1 - Winding	87.5	84.6
InnoSwitch3-Pro, U1	92	86.2
SR FET, Q2	83.2	81.7
Output Capacitor	81.5	78.5

Figure 36 – Enclosed unit thermal performance at 90 VAC / 265VAC, room temperature.

13.1.2 Output: 15 V / 3 A (90 VAC /265 VAC), Ambient Temperature: 25 °C

Component	Temperature (°C)	
	15 V / 3 A @ 90 VAC	15 V / 3 A @ 265 VAC
Case	58.1	54.8
Bridge Rectifier, BR1	93.9	68.6
Bulk Capacitor, C2	84.8	69.8
Transformer, T1 - Core	86.2	83.6
Transformer, T1 - Winding	90	86.8
InnoSwitch3-Pro, U1	93	85.5
SR FET, Q2	87.6	85.4
Output Capacitor	84.5	81

Figure 37 – Enclosed unit thermal performance at 90 VAC / 265VAC, room temperature.

13.1.3 Output: 20 V / 2.25 A (90 VAC /265 VAC), Ambient Temperature: 40 °C

Component	Temperature (°C)	
	20 V / 2.25 A @ 90 VAC	20 V / 2.25 A @ 265 VAC
Case	73	69.5
Bridge Rectifier, BR1	108	83.2
Bulk Capacitor, C2	99.1	84.3
Transformer, T1 - Core	100.6	97.9
Transformer, T1 - Winding	102.7	99.4
InnoSwitch3-Pro, U1	108.3	103.2
SR FET, Q2	98.3	96.3
Output Capacitor	96.5	93.1

Figure 38 – Enclosed Unit Thermal Performance at 90 VAC / 265 VAC, at 40 °C Ambient Temperature.

13.1.4 Output: 15 V / 3 A (90 VAC / 265 VAC), Ambient Temperature: 40 °C

Component	Temperature (°C)	
	15 V / 3 A @ 90 VAC	15 V / 3 A @ 265 VAC
Case	72.7	68.8
Bridge Rectifier, BR1	107.9	83.4
Bulk Capacitor, C2	99.3	84.7
Transformer, T1 - Core	100.9	98.9
Transformer, T1 - Winding	104.9	102.1
InnoSwitch3-Pro, U1	108.1	101
SR FET, Q2	102.7	100.6
Output Capacitor	99.3	96.1

Figure 39 – Enclosed Unit Thermal Performance at 90 VAC / 265 VAC, at 40 °C Ambient Temperature.

14 Waveforms

Note: Measurements taken at room temperature (approximately 24 °C)

14.1 Start-up Waveforms

14.1.1 Output Voltage and Current

Note: Output voltages captured on the board at output connector

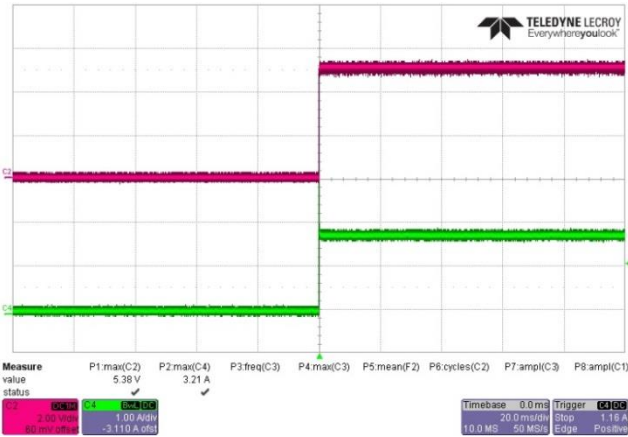


Figure 40 – Output Voltage and Current.
90 VAC, 5.0 V, 3 A Load .
CH2: V_{OUT} , 2 V / div.
CH4: I_{LOAD} , 1 A / div.
Time: 20 ms / div.

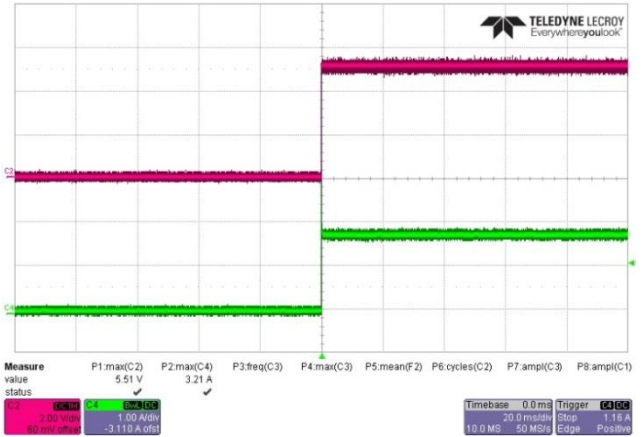


Figure 41 – Output Voltage and Current.
265 VAC, 5.0 V, 3 A Load.
CH2: V_{OUT} , 2 V / div.
CH4: I_{LOAD} , 1 A / div.
Time: 20 ms / div.

14.1.2 Primary Drain Voltage and Current

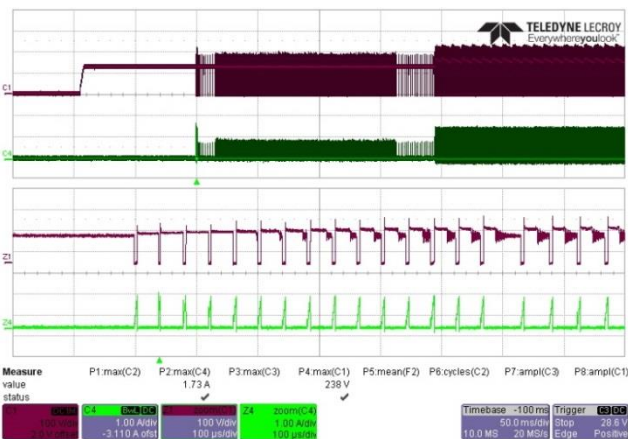


Figure 42 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 3 A Load (238 V_{MAX}).
CH1: V_{DRAIN} , 100 V / div.
CH4: I_{DRAIN} , 1 A / div.
Time: 50 ms / div. (100 μ s / div. Zoom)

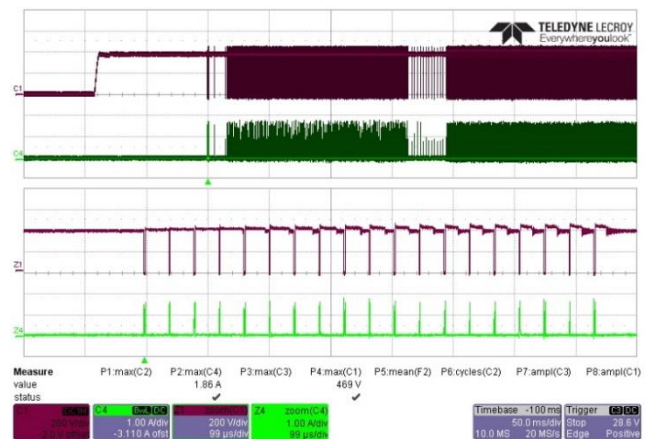


Figure 43 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 3 A Load (469 V_{MAX}).
CH1: V_{DRAIN} , 200 V / div.
CH4: I_{DRAIN} , 1 A / div.
Time: 50 ms / div. (100 μ s / div. Zoom)

14.1.3 SR FET Drain Voltage and Load Current

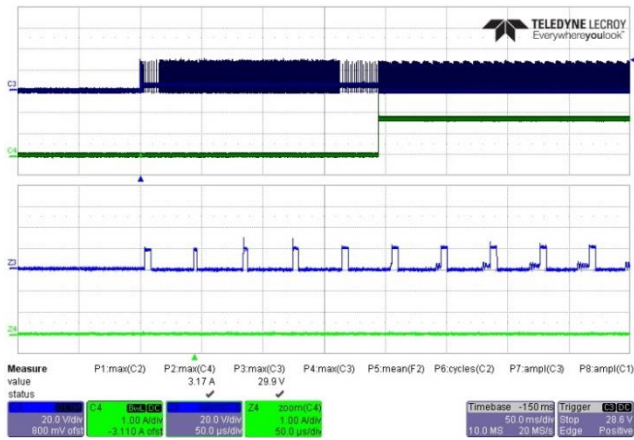


Figure 44 – SR FET Drain Voltage and Load Current.
 90 VAC, 5.0 V, 3 A Load (29.9 V_{MAX}).
 CH3: V_{DRAIN(SR)}, 20 V / div.
 CH4: I_{Load}, 1 A / div.
 Time: 50 ns / div. (50 μs / div. Zoom)

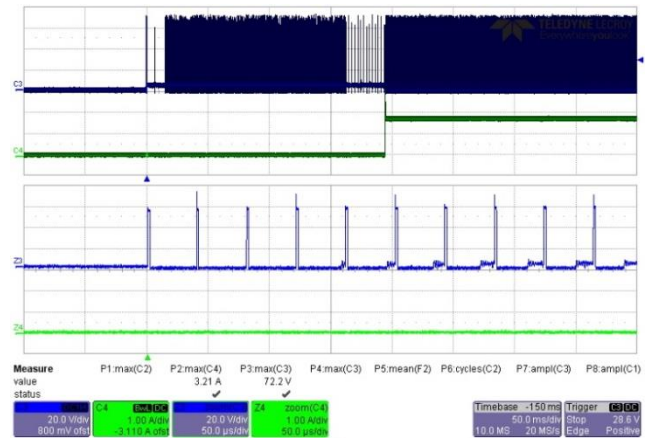


Figure 45 – SR FET Drain Voltage and Load Current.
 265 VAC, 5.0 V, 3 A Load (72.2 V_{MAX}).
 CH3: V_{DRAIN(SR)}, 20 V / div.
 CH4: I_{Load}, 1 A / div.
 Time: 50 ns / div. (50 μs / div. Zoom)

14.2 Load Transient Response

Note: Output voltages captured at the end of 100 mΩ cable

14.2.1 Output: 5 V / 3 A

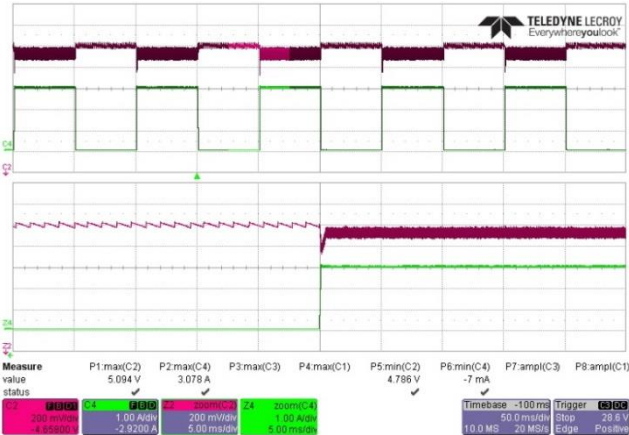


Figure 46 – Transient Response.
 90 VAC, 5.0 V, 0 – 3 A Load Step.
 V_{MIN} : 4.786 V, V_{MAX} : 5.094 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

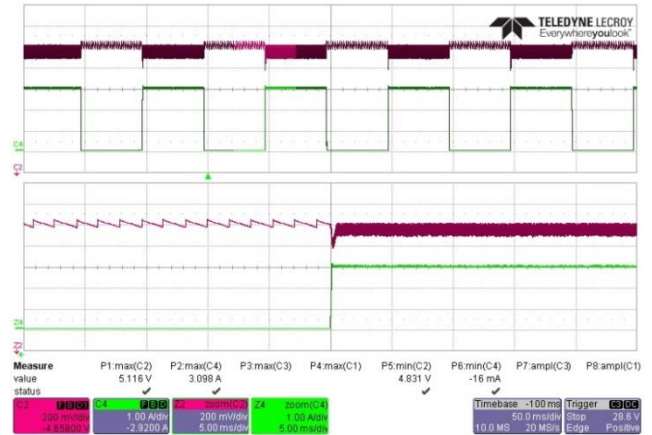


Figure 47 – Transient Response.
 265 VAC, 5.0 V, 0 – 3 A Load Step.
 V_{MIN} : 4.831 V, V_{MAX} : 5.116 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

14.2.2 Output: 9 V / 3 A

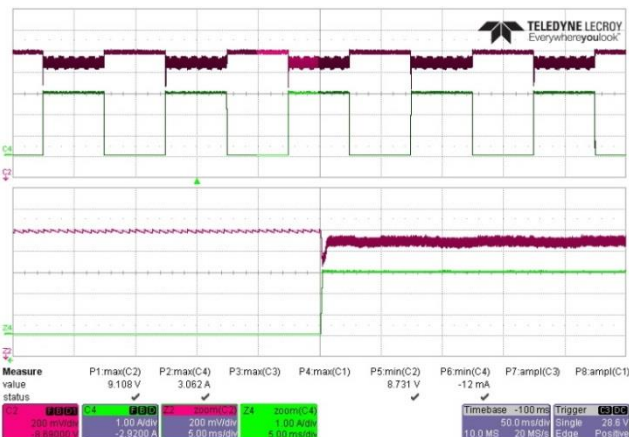


Figure 48 – Transient Response.
 90 VAC, 9.0 V, 0 – 3 A Load Step.
 V_{MIN} : 8.731 V, V_{MAX} : 9.108 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

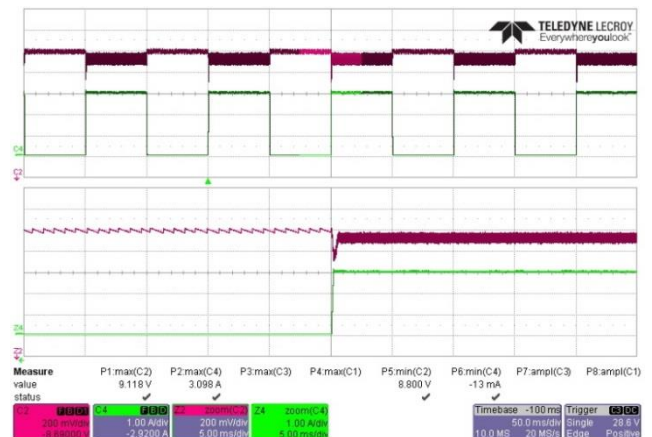


Figure 49 – Transient Response.
 265 VAC, 9.0 V, 0 – 3 A Load Step.
 V_{MIN} : 8.800 V, V_{MAX} : 9.118 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

14.2.3 Output: 15 V / 3 A

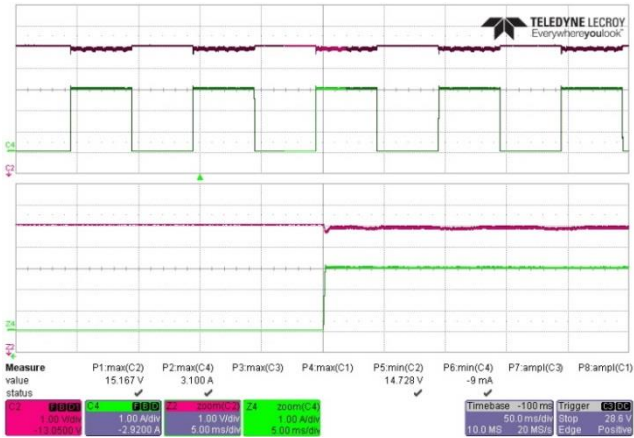


Figure 50 – Transient Response.
 90 VAC, 15.0 V, 0 – 3 A Load Step.
 V_{MIN} : 14.728 V, V_{MAX} : 15.167 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

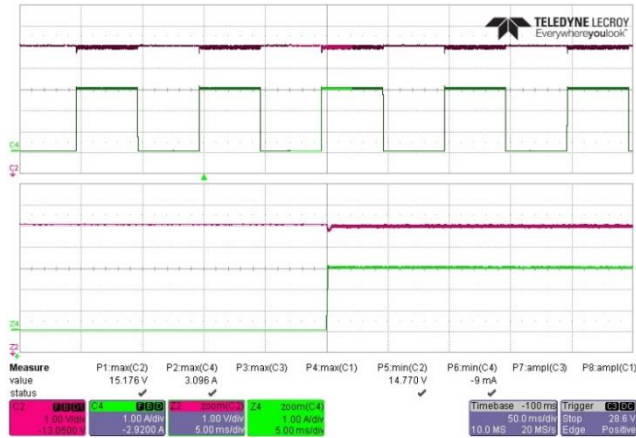


Figure 51 – Transient Response.
 265 VAC, 15.0 V, 0 – 3 A Load Step.
 V_{MIN} : 14.770 V, V_{MAX} : 15.176 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

14.2.4 Output: 20 V / 2.25 A

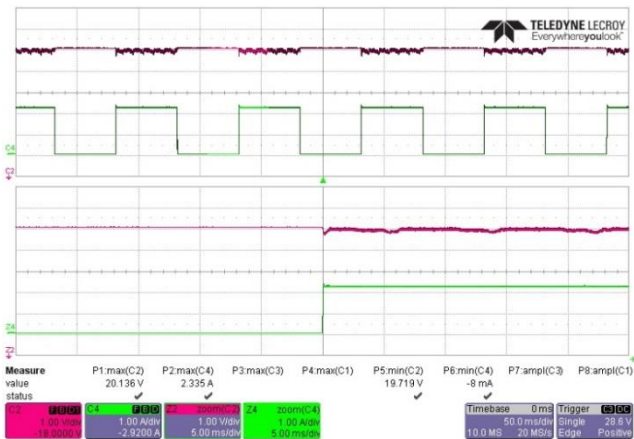


Figure 52 – Transient Response.
 90 VAC, 20.0 V, 0 – 2.25 A Load Step.
 V_{MIN} : 19.719 V, V_{MAX} : 20.136 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

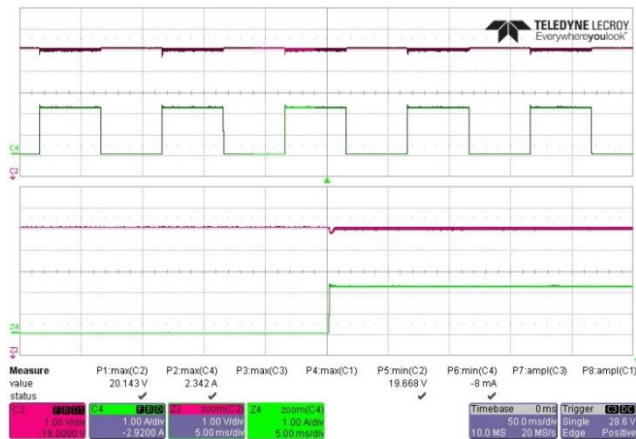


Figure 53 – Transient Response.
 265 VAC, 20.0 V, 0 – 2.25 A Load Step.
 V_{MIN} : 19.668 V, V_{MAX} : 20.143 V.
 CH2: V_{OUT} , 0.2 V / div.
 CH4: I_{LOAD} , 1 A / div.
 Time: 50 ms / div. (5 ms / div. Zoom)

14.3 Primary Drain Voltage and Current (Steady-State)

14.3.1 Output: 5 V / 3 A

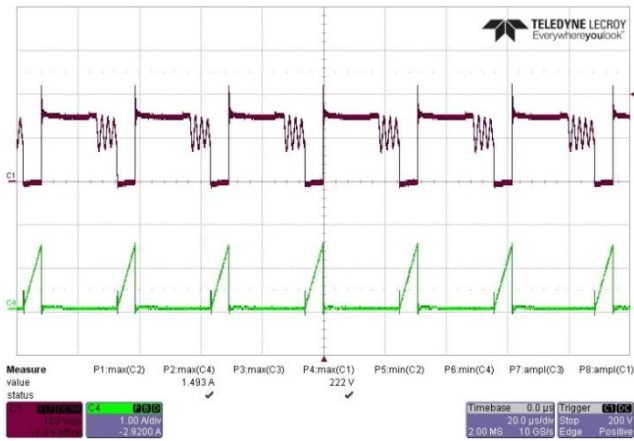


Figure 54 – Primary Drain Voltage and Current.
 90 VAC, 5.0 V, 3 A Load (222 V_{MAX}).
 CH: V_{DRAIN}, 100 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

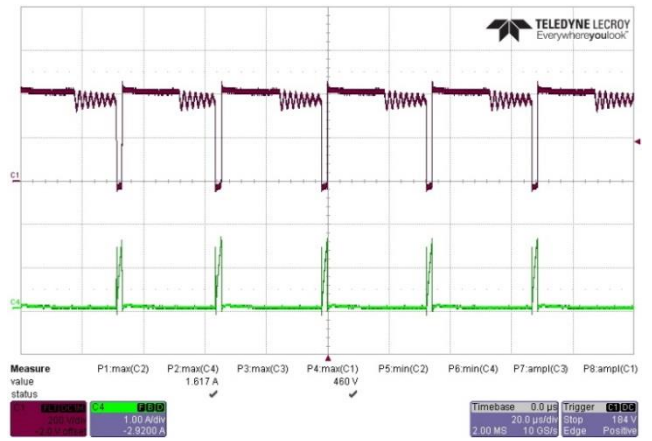


Figure 55 – Primary Drain Voltage and Current.
 265 VAC, 5.0 V, 3 A Load (460 V_{MAX}).
 CH: V_{DRAIN}, 200 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

14.3.2 Output: 9 V / 3 A

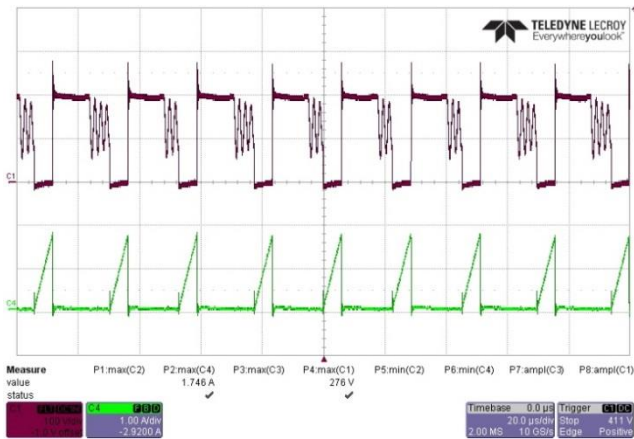


Figure 56 – Primary Drain Voltage and Current.
 90 VAC, 9.0 V, 3 A Load (276 V_{MAX}).
 CH: V_{DRAIN}, 100 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

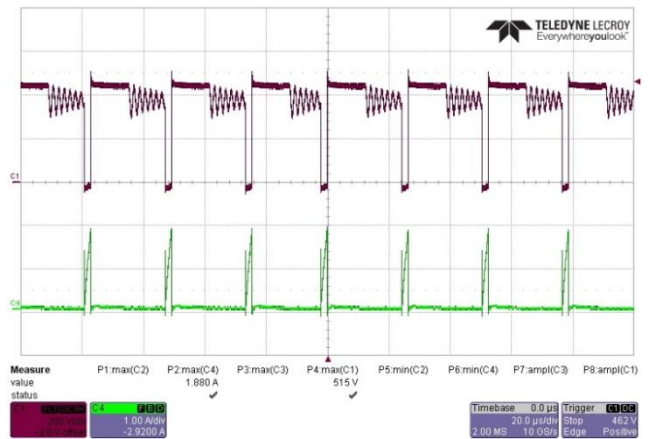


Figure 57 – Primary Drain Voltage and Current.
 265 VAC, 9.0 V, 3 A Load (515 V_{MAX}).
 CH: V_{DRAIN}, 200 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

14.3.3 Output: 15 V / 3 A

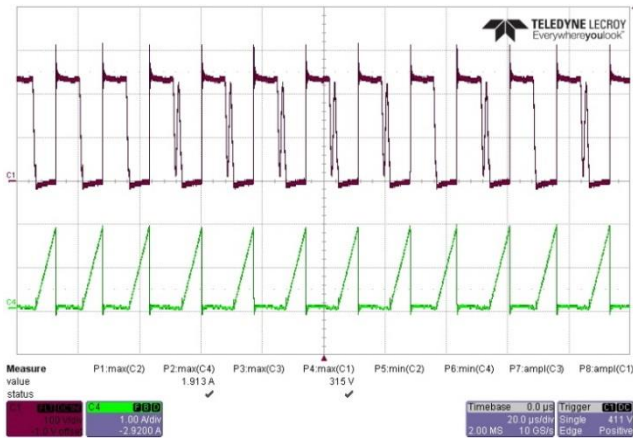


Figure 58 – Primary Drain Voltage and Current.
 90 VAC, 15.0 V, 3 A Load (315 V_{MAX}).
 CH: V_{DRAIN}, 100 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

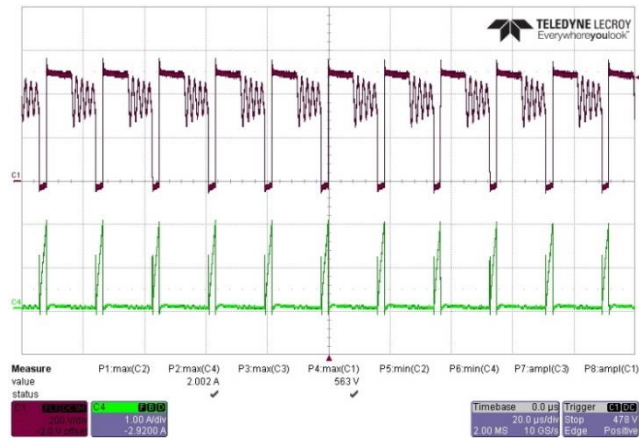


Figure 59 – Primary Drain Voltage and Current.
 265 VAC, 15.0 V, 3 A Load (563 V_{MAX}).
 CH: V_{DRAIN}, 200 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

14.3.4 Output: 20 V / 2.25 A

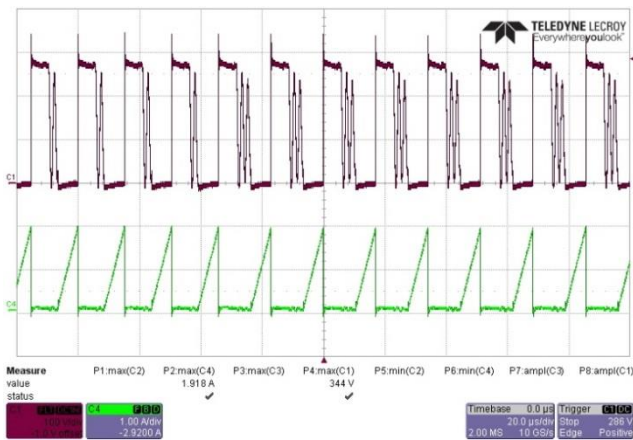


Figure 60 – Primary Drain Voltage and Current.
 90 VAC, 20.0 V, 2.25 A Load (344 V_{MAX}).
 CH: V_{DRAIN}, 100 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

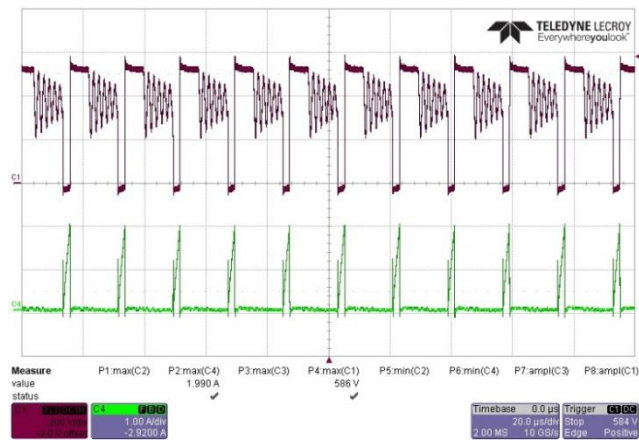


Figure 61 – Primary Drain Voltage and Current.
 265 VAC, 20.0 V, 2.25 A Load (586 V_{MAX}).
 CH: V_{DRAIN}, 200 V / div.
 CH4: I_{DRAIN}, 1 A / div.
 Time: 20 μs / div.

14.4 SR FET Drain Voltage and Load Current (Steady-State)

14.4.1 Output: 5 V / 3 A

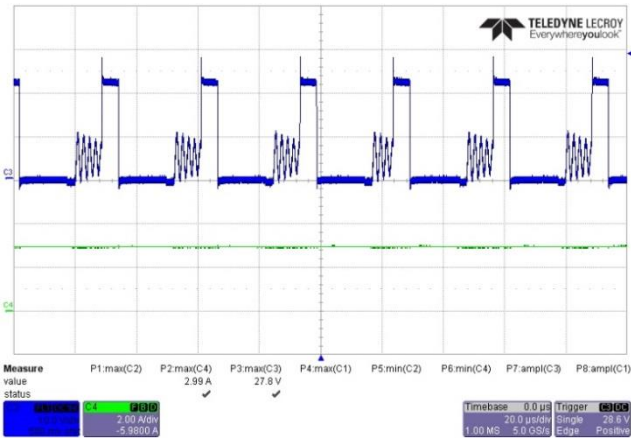


Figure 62 – SR FET Drain Voltage and Current.
 90 VAC, 5.0 V, 3 A Load (27.8 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 10 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 µs / div.

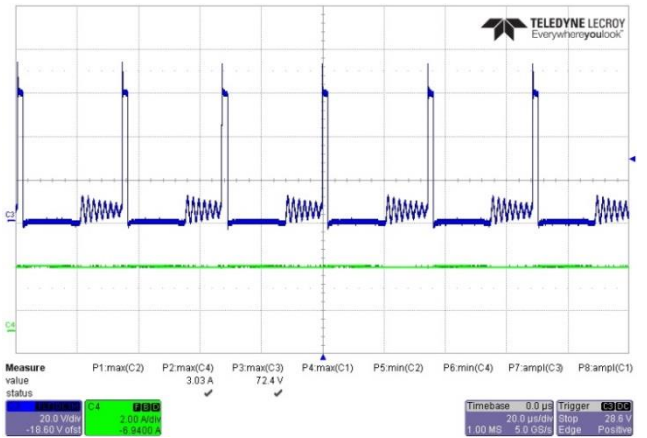


Figure 63 – SR FET Drain Voltage and Current.
 265 VAC, 5.0 V, 3 A Load (72.4 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 20 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 µs / div.

14.4.2 Output: 9 V / 3 A

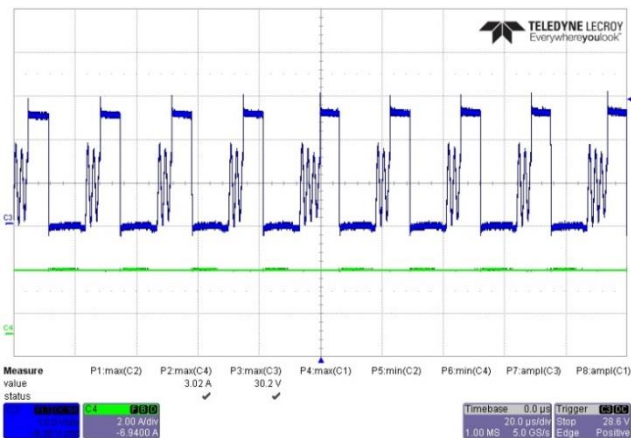


Figure 64 – SR FET Drain Voltage and Current.
 90 VAC, 9.0 V, 3 A Load (30.2 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 10 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 µs / div.

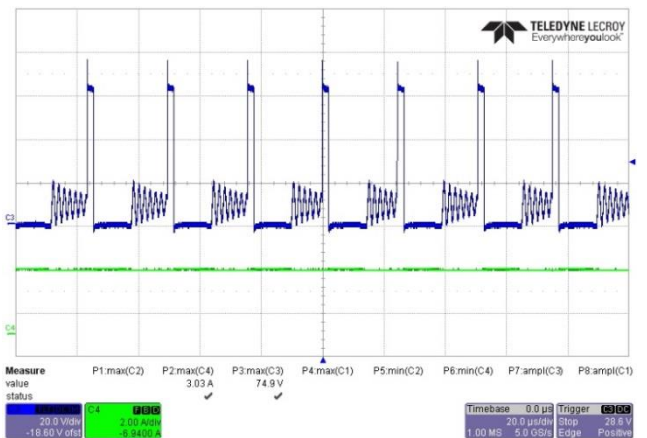


Figure 65 – SR FET Drain Voltage and Current.
 265 VAC, 9.0 V, 3 A Load (74.9 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 20 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 µs / div.



14.4.3 Output: 15 V / 3 A

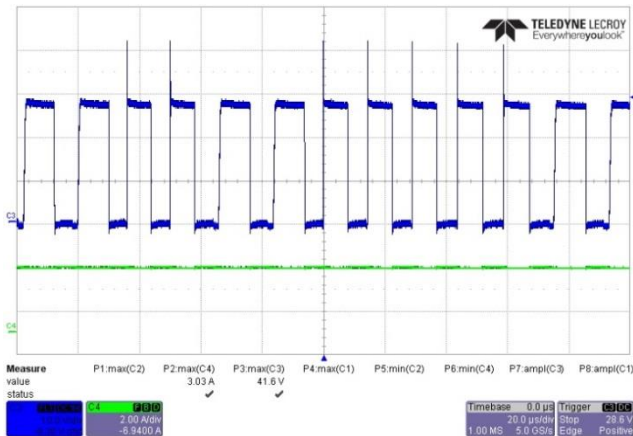


Figure 66 – SR FET Drain Voltage and Current.
 90 VAC, 15.0 V, 3 A Load (41.6 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 10 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 μs / div.

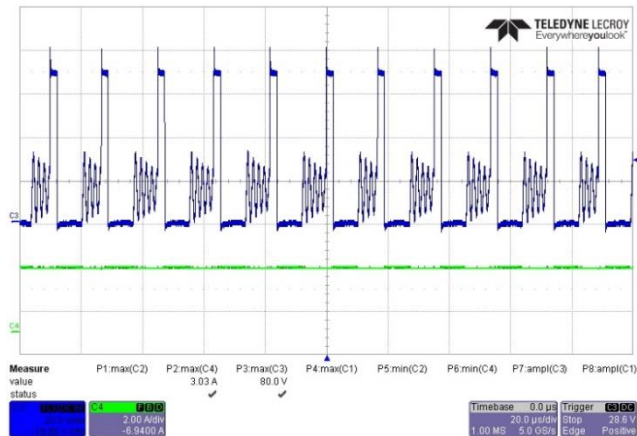


Figure 67 – SR FET Drain Voltage and Current.
 265 VAC, 15.0 V, 3 A Load (80 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 20 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 μs / div.

14.4.4 Output: 20 V / 2.25 A

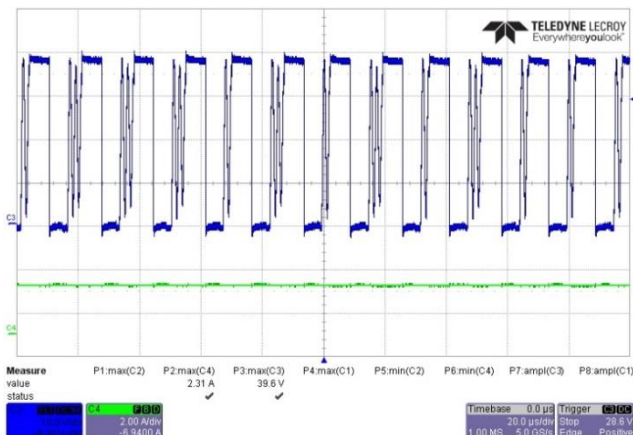


Figure 68 – SR FET Drain Voltage and Current.
 90 VAC, 20.0 V, 3 A Load (39.6 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 10 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 μs / div.

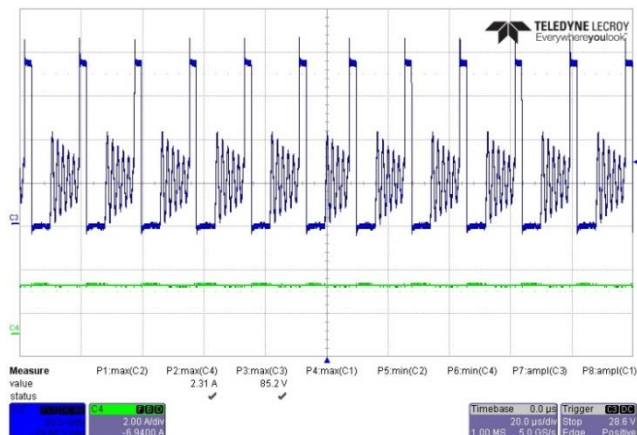


Figure 69 – SR FET Drain Voltage and Current.
 85 VAC, 20.0 V, 3 A Load (85.2 V_{MAX}).
 CH4: V_{DRAIN(SR)}, 20 V / div.
 CH1: I_{DRAIN(SR)}, 2 A / div.
 Time: 20 μs / div.

15 Output Ripple Measurements

15.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 $\mu\text{F}/50\text{ V}$ ceramic type and one (1) 47 $\mu\text{F}/50\text{ V}$ aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

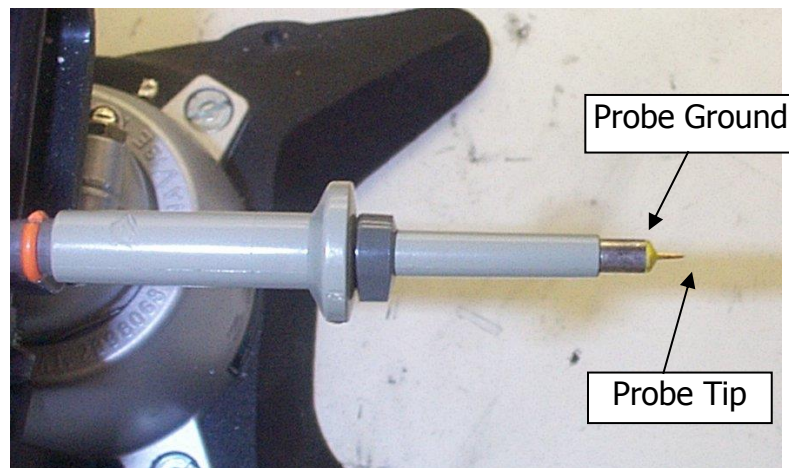


Figure 70 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 71 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added).

15.2 Output Voltage Ripple Waveforms

- Note 1:** Output voltages captured at the end of 100 mΩ cable
- Note 2:** Measurements taken at room temperature (approximately 24 °C)

15.2.1 Output: 5 V / 3 A

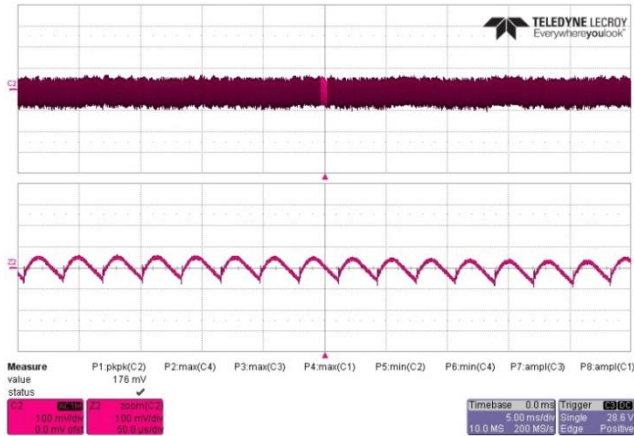


Figure 72 – Output Voltage Ripple.
 90 VAC, 5.0 V, 3 A Load (176 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

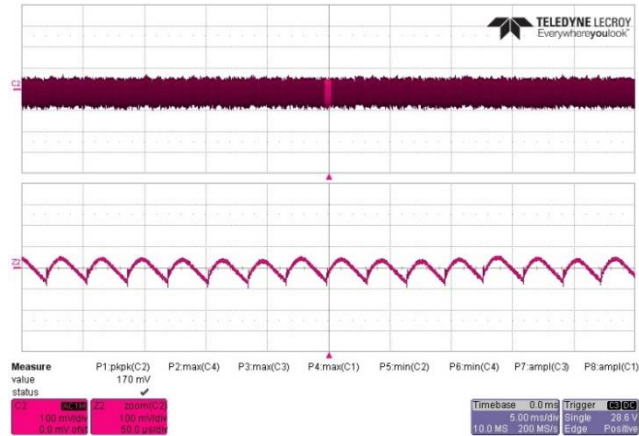


Figure 73 – Output Voltage Ripple.
 115 VAC, 5.0 V, 3 A Load (170 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

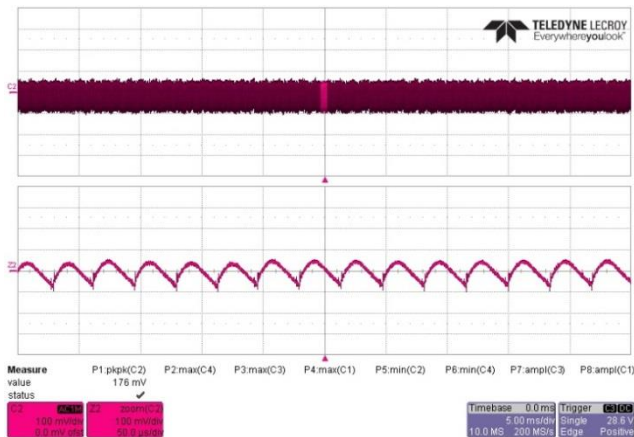


Figure 74 – Output Voltage Ripple.
 230 VAC, 5.0 V, 3 A Load (176 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

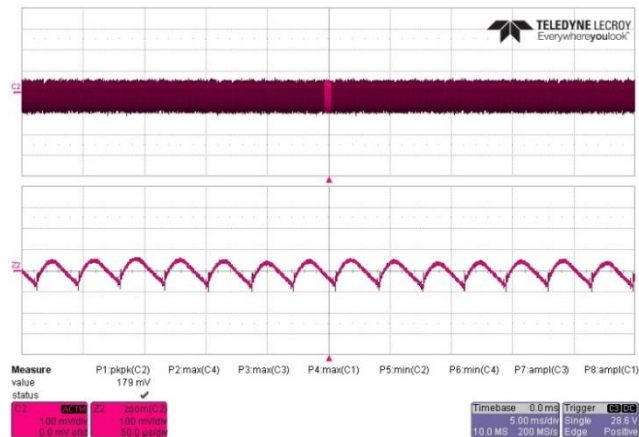


Figure 75 – Output Voltage Ripple.
 265 VAC, 5.0 V, 3 A Load (179 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

15.2.2 Output: 9 V / 3 A

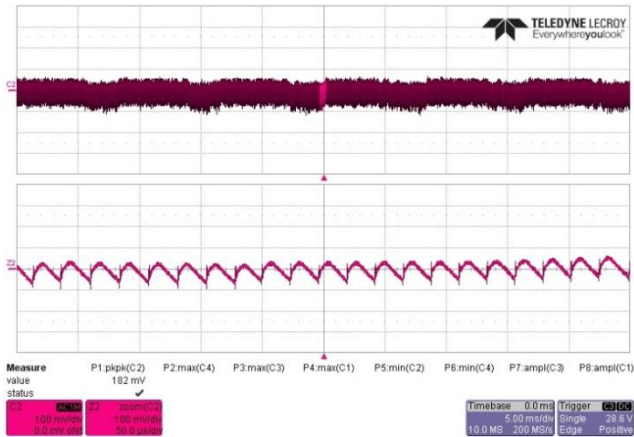


Figure 76 – Output Voltage Ripple.
 90 VAC, 9.0 V, 3 A Load (182 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

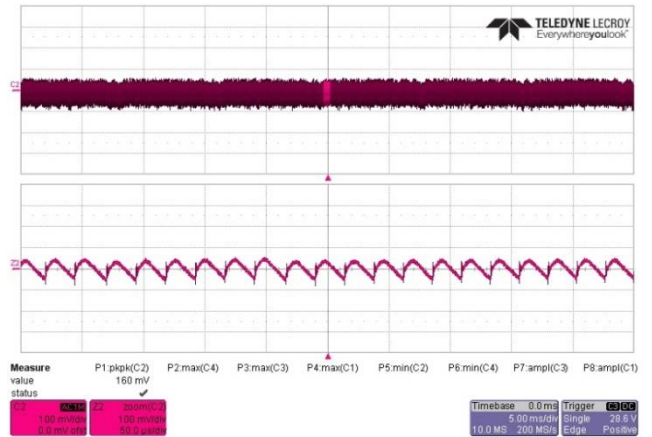


Figure 77 – Output Voltage Ripple.
 115 VAC, 9.0 V, 3 A Load (160 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

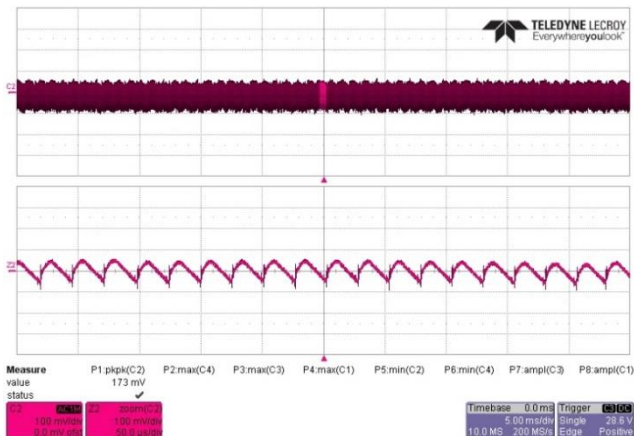


Figure 78 – Output Voltage Ripple.
 230 VAC, 9.0 V, 3 A Load (173 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

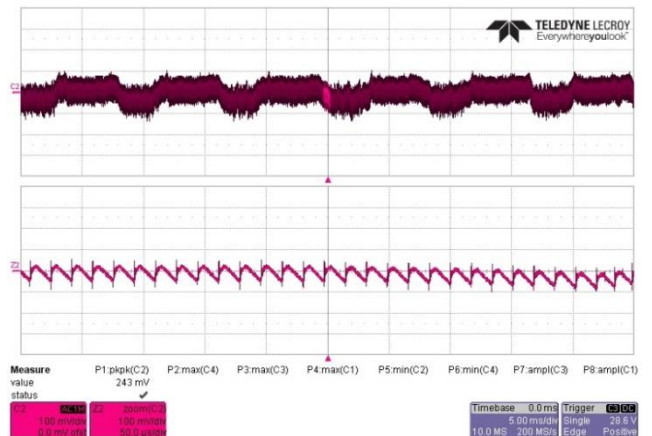


Figure 79 – Output Voltage Ripple.
 265 VAC, 9.0 V, 3 A Load (243 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

15.2.3 Output: 15 V / 3 A

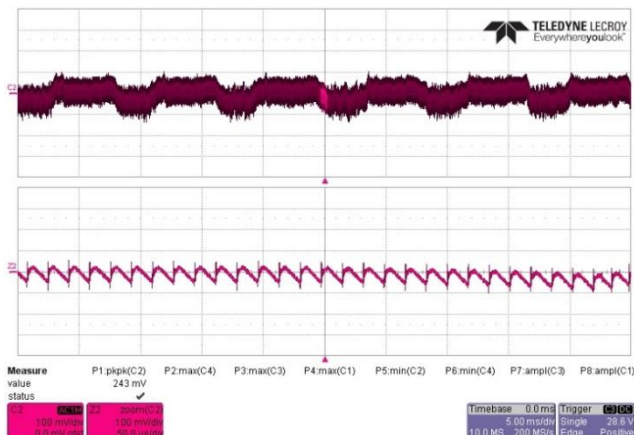


Figure 80 – Output Voltage Ripple.
 90 VAC, 15.0 V, 3 A Load (243 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

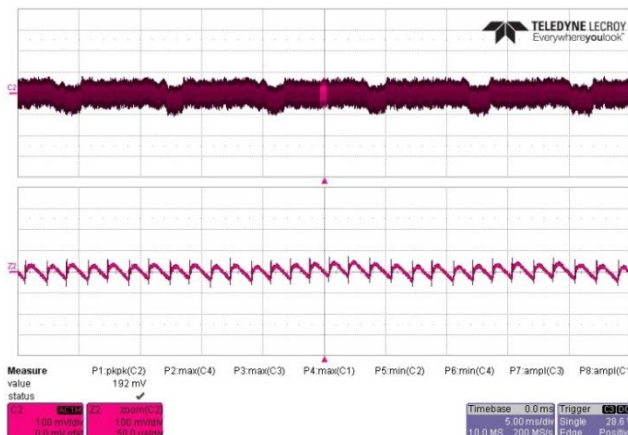


Figure 81 – Output Voltage Ripple.
 115 VAC, 15.0 V, 3 A Load (192 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

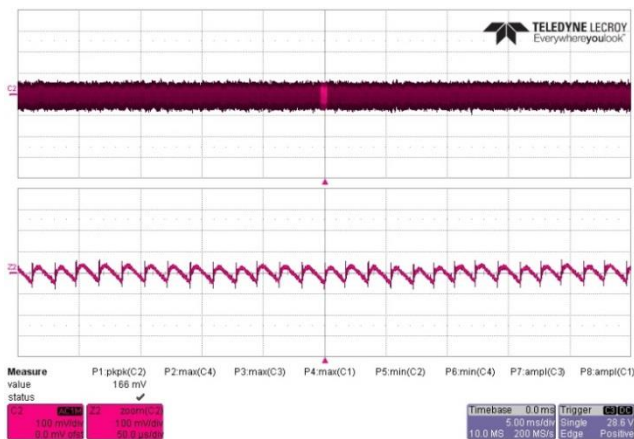


Figure 82 – Output Voltage Ripple.
 230 VAC, 15.0 V, 3 A Load (166 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

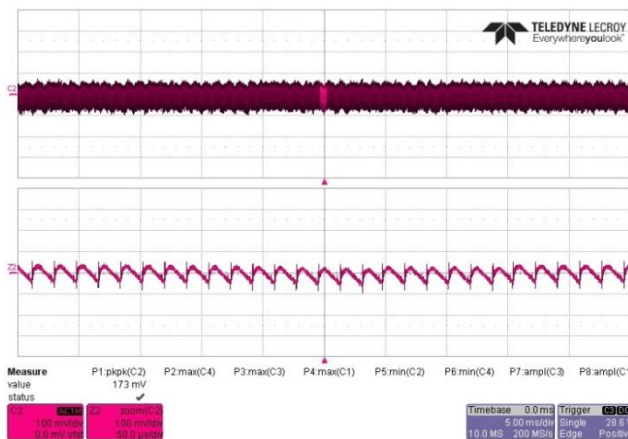


Figure 83 – Output Voltage Ripple.
 265 VAC, 15.0 V, 3 A Load (173 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

15.2.4 Output: 20 V / 2.25 A

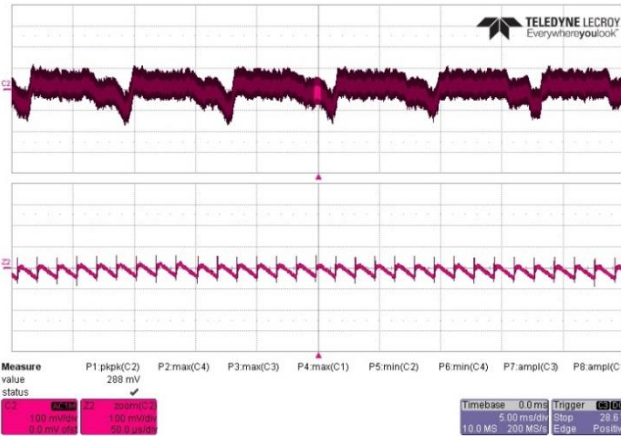


Figure 84 – Output Voltage Ripple.
 90 VAC, 20.0 V, 2.25 A Load (288 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

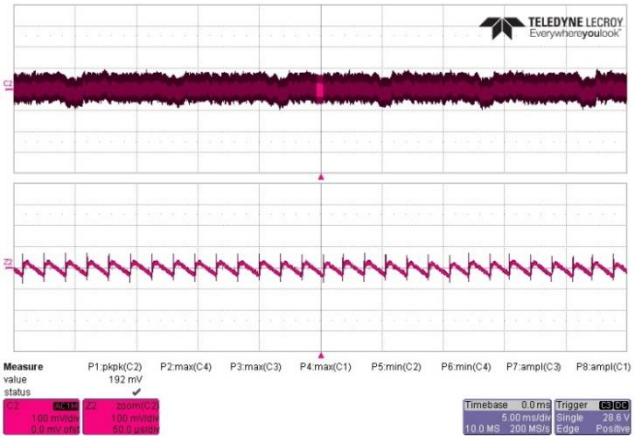


Figure 85 – Output Voltage Ripple.
 115 VAC, 20.0 V, 2.25 A Load (192 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

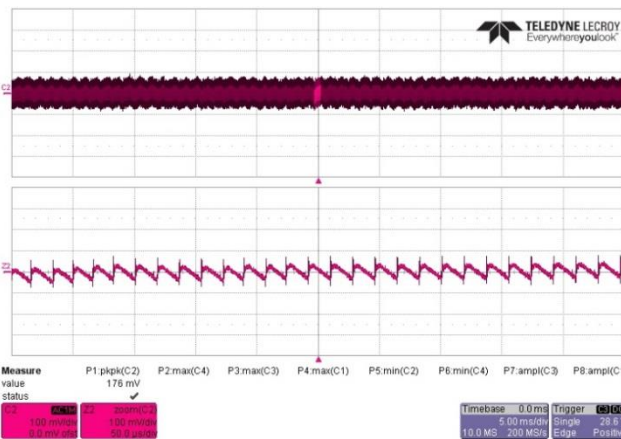


Figure 86 – Output Voltage Ripple.
 230 VAC, 20.0 V, 2.25 A Load (176 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

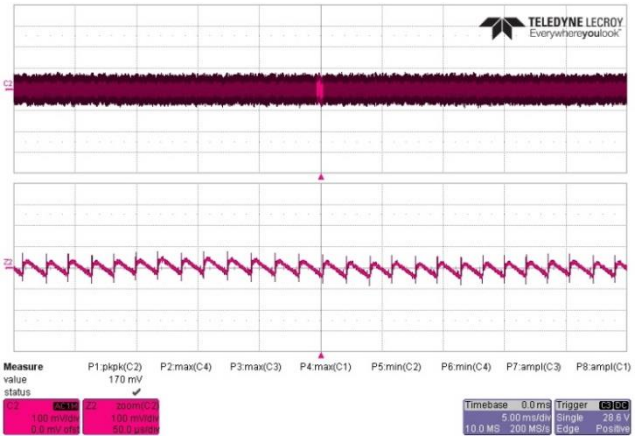


Figure 87 – Output Voltage Ripple.
 265 VAC, 20.0 V, 2.25 A Load (170 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (50 μs / div. Zoom)

15.2.5 Output: 5 V / 0 A

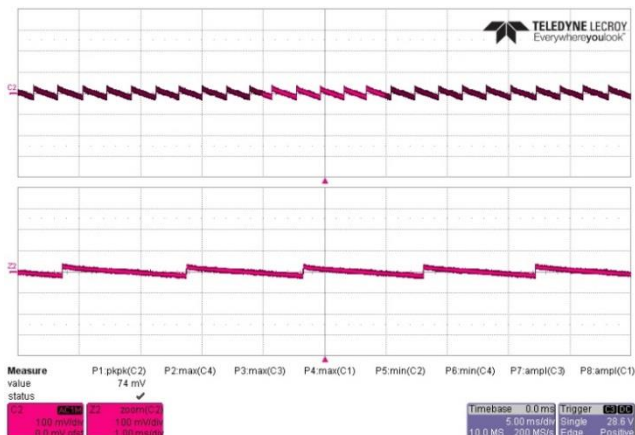


Figure 88 – Output Voltage Ripple.
 90 VAC, 5.0 V, 0 A Load (74 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

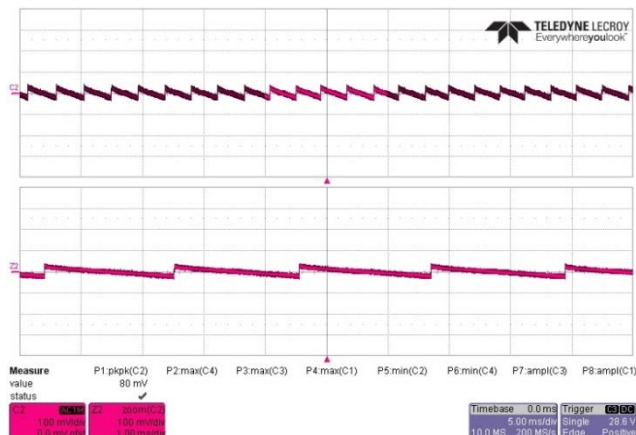


Figure 89 – Output Voltage Ripple.
 115 VAC, 5.0 V, 0 A Load (80 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

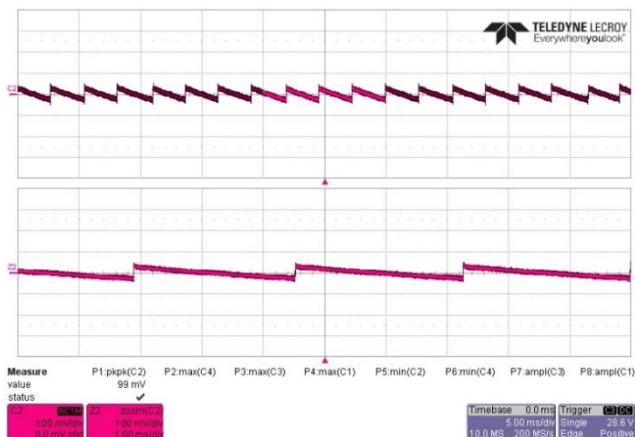


Figure 90 – Output Voltage Ripple.
 230 VAC, 5.0 V, 0 A Load (99 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

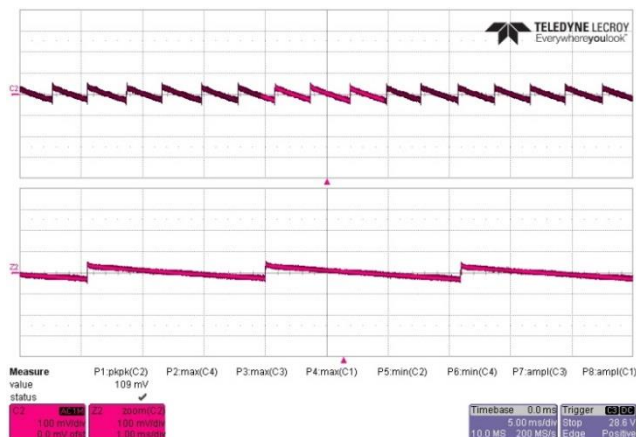


Figure 91 – Output Voltage Ripple.
 265 VAC, 5.0 V, 0 A Load (109 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

15.2.6 Output: 9 V / 0 A

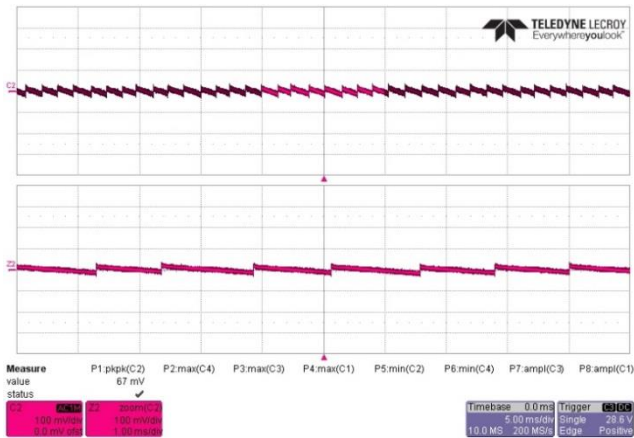


Figure 92 – Output Voltage Ripple.
 90 VAC, 9.0 V, 0 A Load (67 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

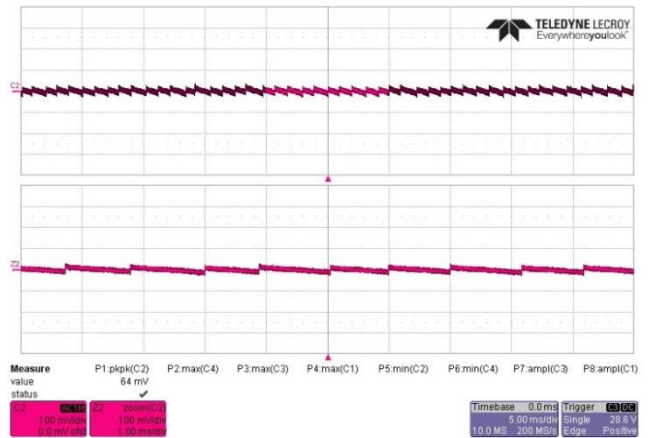


Figure 93 – Output Voltage Ripple.
 115 VAC, 9.0 V, 0 A Load (64 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

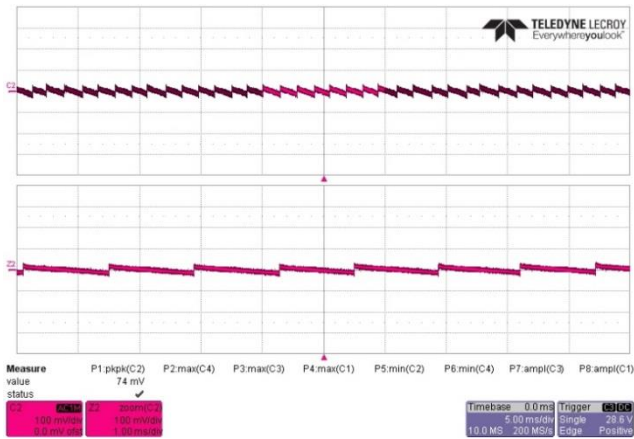


Figure 94 – Output Voltage Ripple.
 230 VAC, 9.0 V, 0 A Load (74 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

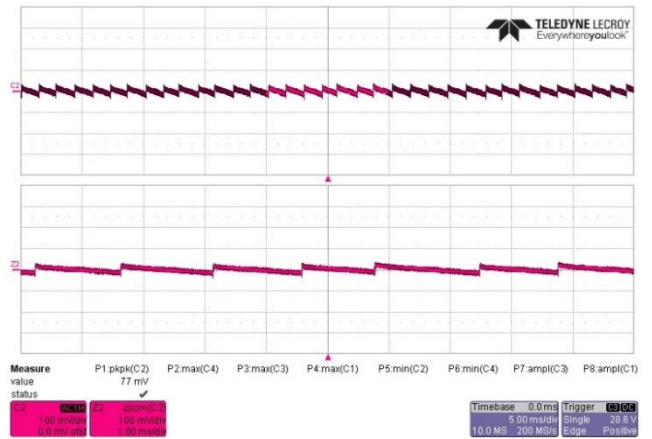


Figure 95 – Output Voltage Ripple.
 265 VAC, 9.0 V, 0 A Load (77 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)



15.2.7 Output: 15 V / 0 A

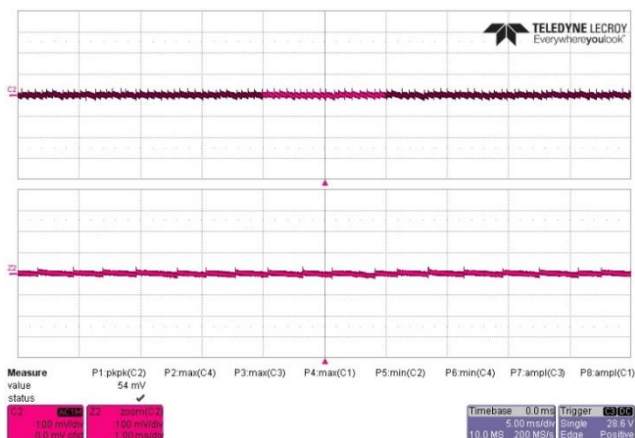


Figure 96 – Output Voltage Ripple.
 90 VAC, 15.0 V, 0 A Load (54 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

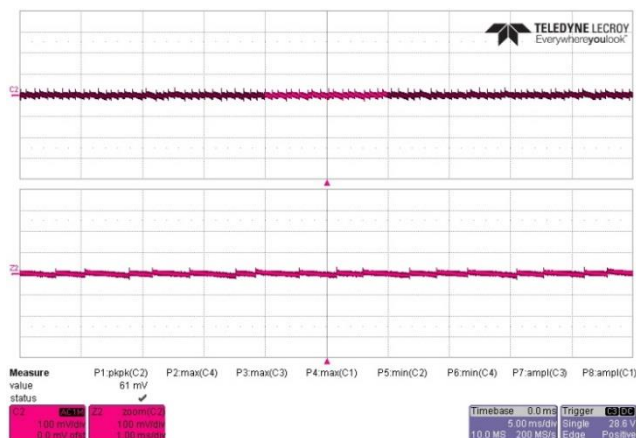


Figure 97 – Output Voltage Ripple.
 115 VAC, 15.0 V, 0 A Load (61 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

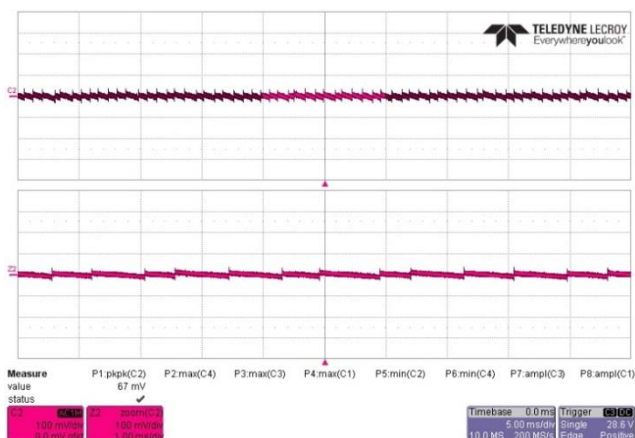


Figure 98 – Output Voltage Ripple.
 230 VAC, 15.0 V, 0 A Load (67 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (1 ms / div. Zoom)

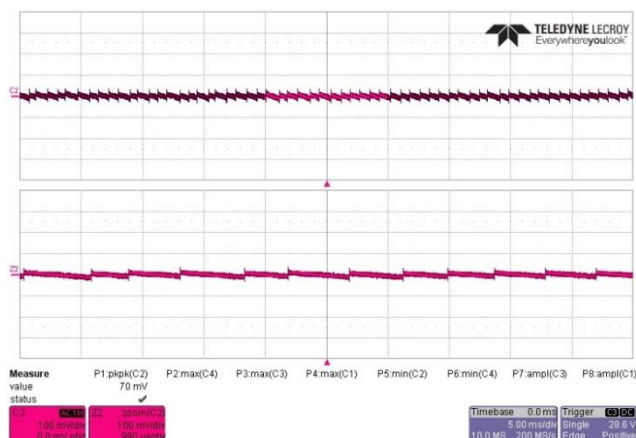


Figure 99 – Output Voltage Ripple.
 265 VAC, 15.0 V, 0 A Load (70 mV_{PK-PK}).
 CH2: V_{OUT(AC)}, 100 mV / div.
 Time: 5 ms / div. (.99 ms / div. Zoom)

15.2.8 Output: 20 V / 0 A

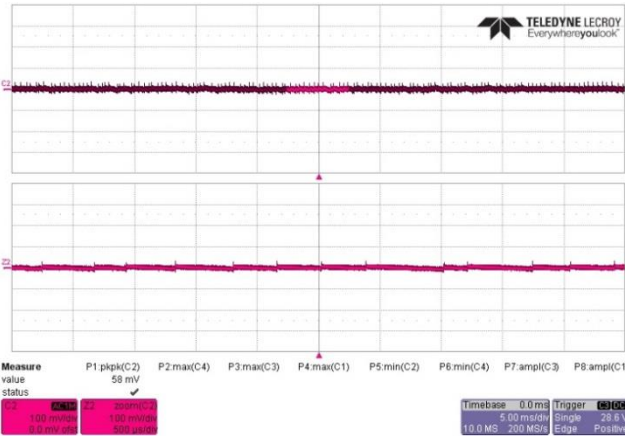


Figure 100 – Output Voltage Ripple.
 90 VAC, 20.0 V, 0A Load (58 mV_{PK-PK}).
 CH2: $V_{OUT(AC)}$, 100 mV / div.
 Time: 5 ms / div. (0.5 ms / div. Zoom)

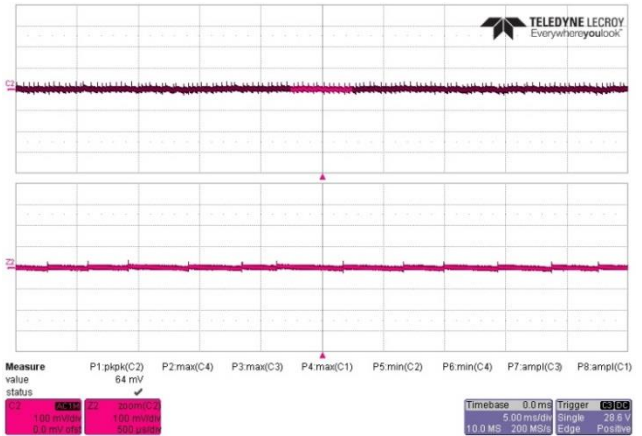


Figure 101 – Output Voltage Ripple.
 115 VAC, 20.0 V, 0 A Load (64 mV_{PK-PK}).
 CH2: $V_{OUT(AC)}$, 100 mV / div.
 Time: 5 ms / div. (0.5 ms / div. Zoom)

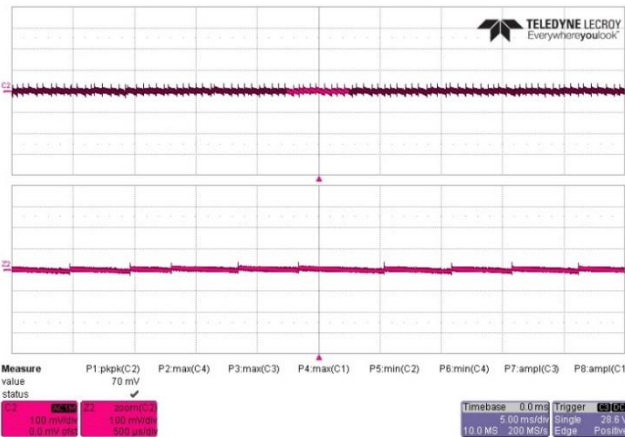


Figure 102 – Output Voltage Ripple.
 230 VAC, 20.0 V, 0 A Load (70 mV_{PK-PK}).
 CH2: $V_{OUT(AC)}$, 100 mV / div.
 Time: 5 ms / div. (0.5 ms / div. Zoom)

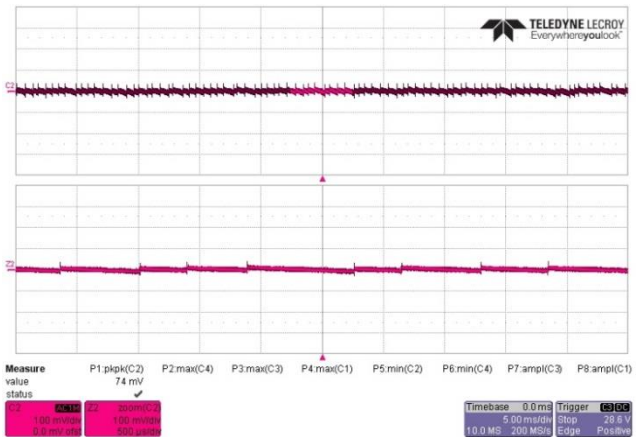
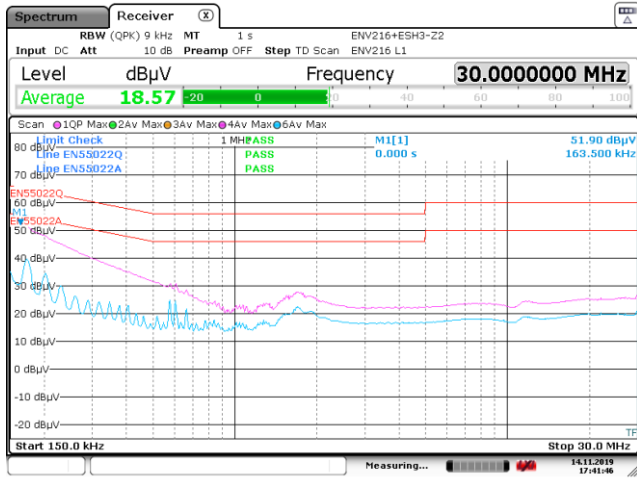


Figure 103 – Output Voltage Ripple.
 265 VAC, 20.0 V, 0 A Load (74 mV_{PK-PK}).
 CH2: $V_{OUT(AC)}$, 100 mV / div.
 Time: 5 ms / div. (0.5 ms / div. Zoom)

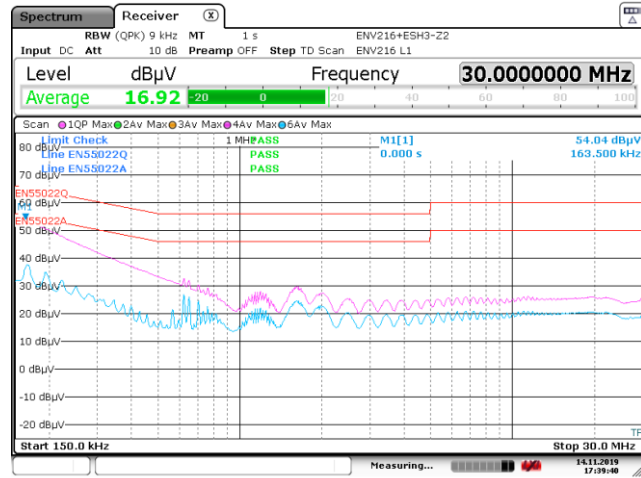
16 Conducted EMI

16.1 Floating Ground (QPK / AV)

16.1.1 Output: 5 V / 3 A



Date: 14.NOV.2019 17:41:46

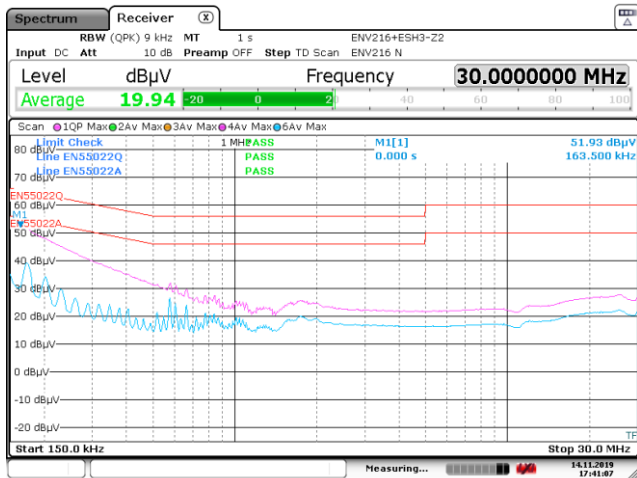


Date: 14.NOV.2019 17:39:40

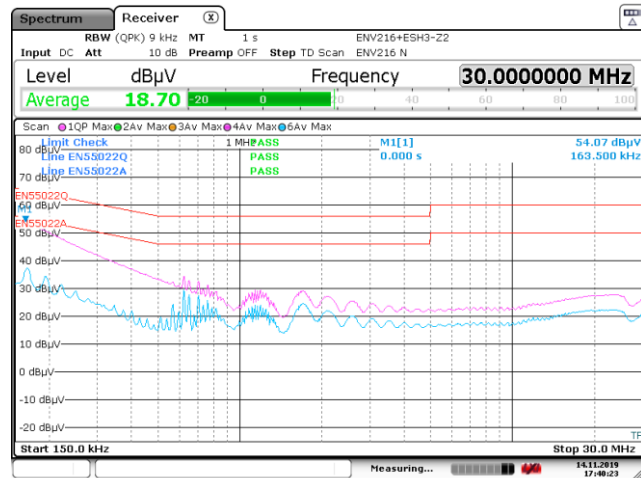
115 VAC.

230 VAC.

Figure 104 – Floating Ground EMI, 5 V / 3 A Load [Line Scan].



Date: 14.NOV.2019 17:41:07



Date: 14.NOV.2019 17:40:23

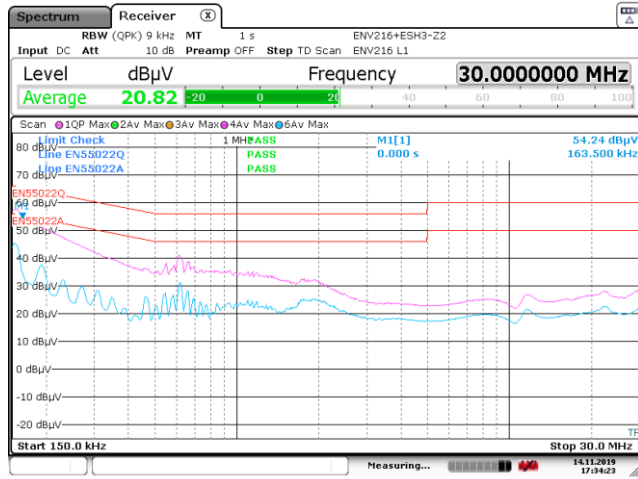
115 VAC.

230 VAC.

Figure 105 – Floating Ground EMI, 5 V / 3 A Load [Neutral Scan].

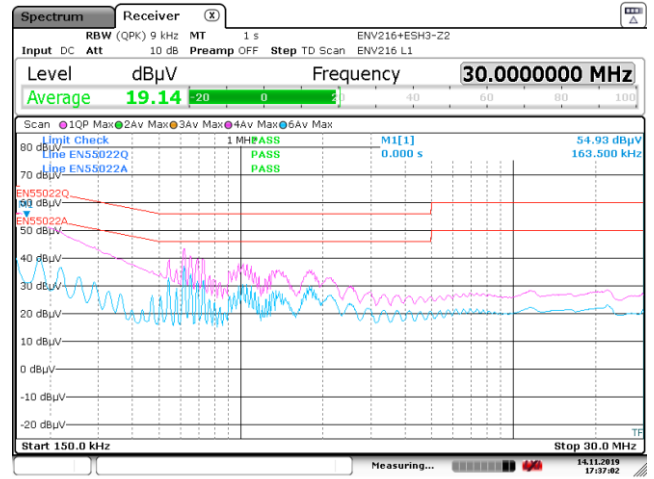


16.1.2 Output: 9 V / 3 A



Date: 14.NOV.2019 17:34:24

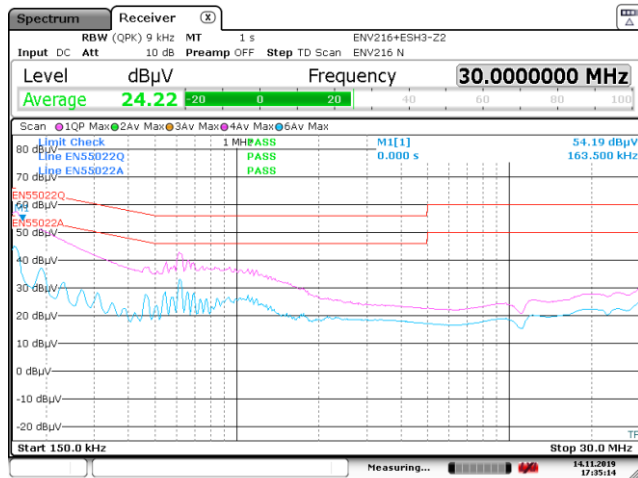
115 VAC.



Date: 14.NOV.2019 17:37:03

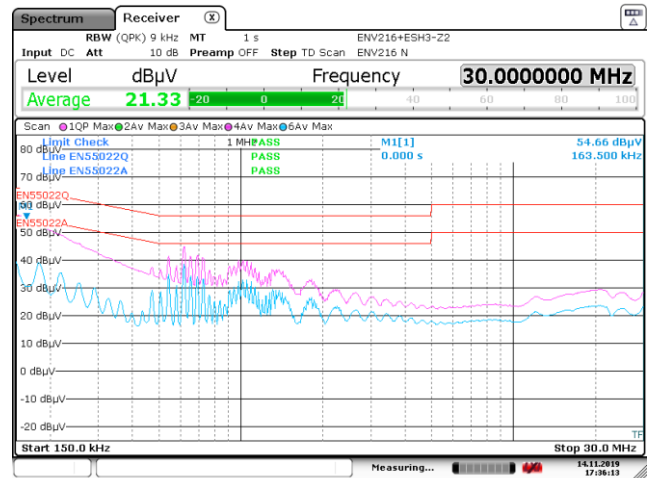
230 VAC.

Figure 106 – Floating Ground EMI, 9 V / 3 A Load [Line Scan].



Date: 14.NOV.2019 17:35:14

115 VAC.



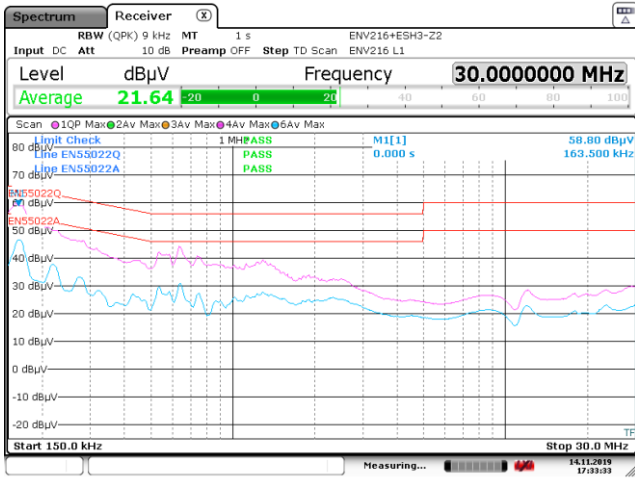
Date: 14.NOV.2019 17:36:14

230 VAC.

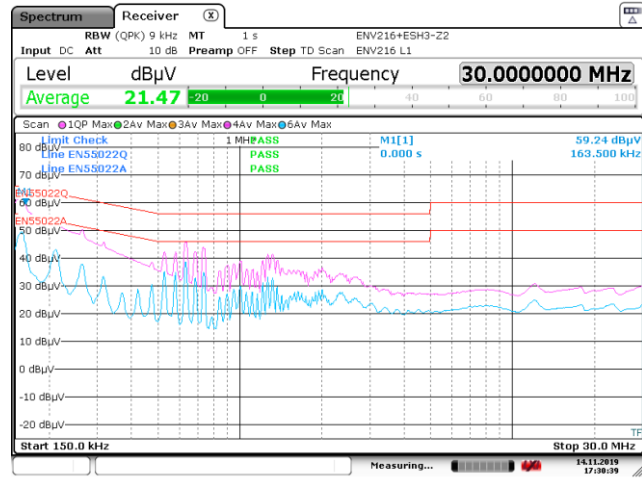
Figure 107 – Floating Ground EMI, 9 V / 3 A Load [Neutral Scan].



16.1.3 Output: 15 V / 3 A



Date: 14.NOV.2019 17:33:33

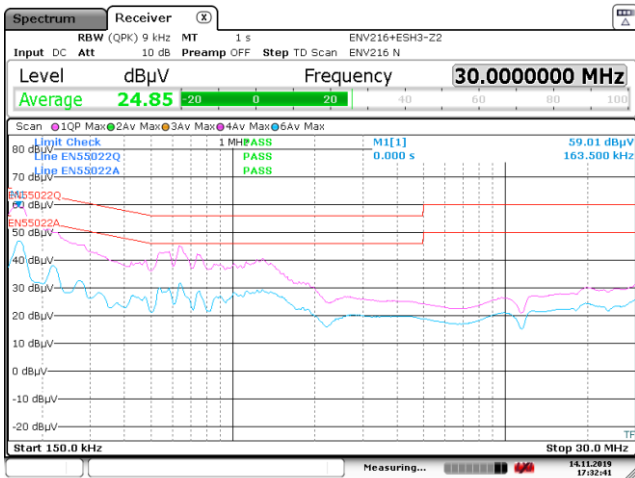


Date: 14.NOV.2019 17:30:39

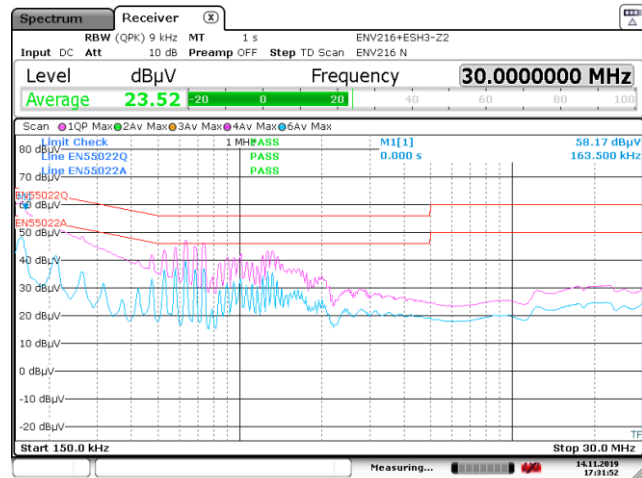
115 VAC.

230 VAC.

Figure 108 – Floating Ground EMI, 15 V / 3 A Load [Line Scan].



Date: 14.NOV.2019 17:32:41



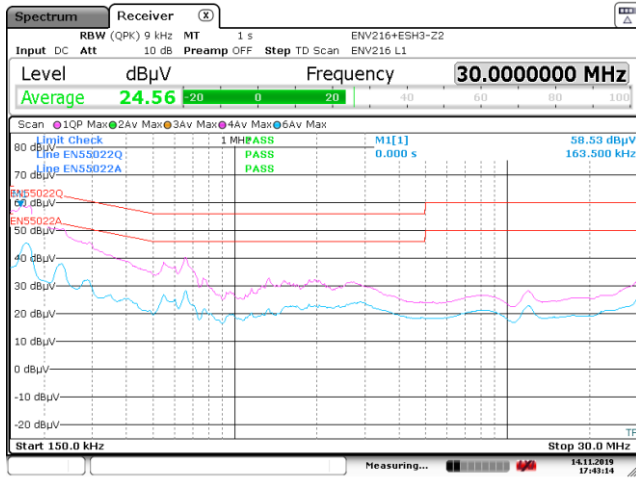
Date: 14.NOV.2019 17:31:52

115 VAC.

230 VAC.

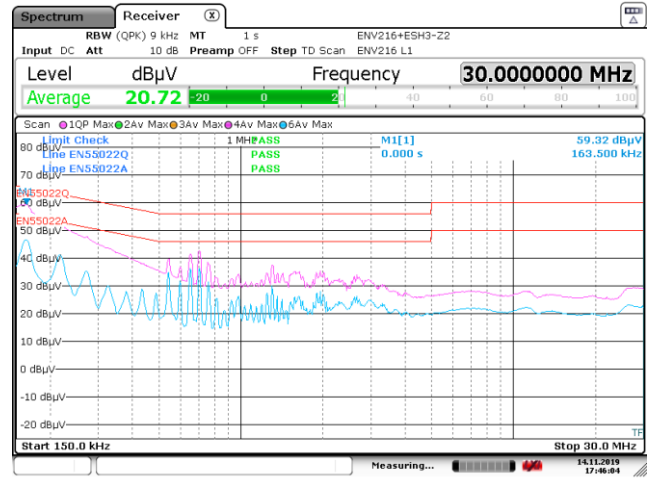
Figure 109 – Floating Ground EMI, 15 V / 3 A Load [Neutral Scan].

16.1.4 Output: 20 V / 2.25 A



Date: 14.NOV.2019 17:43:14

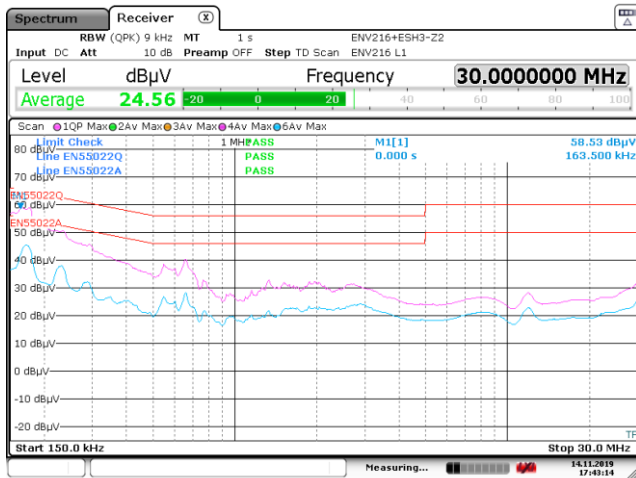
115 VAC.



Date: 14.NOV.2019 17:46:03

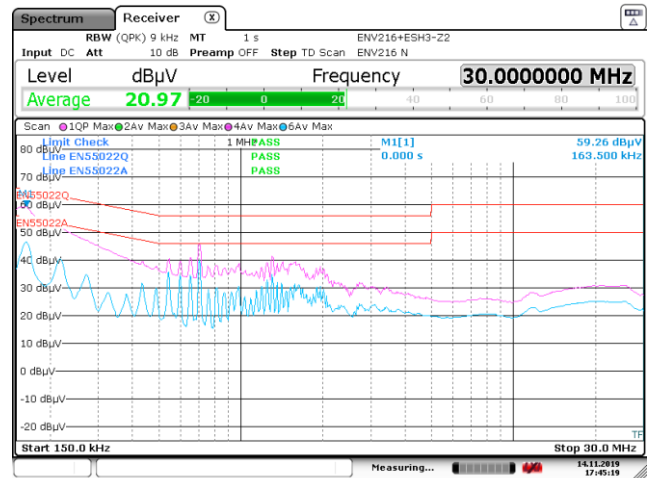
230 VAC.

Figure 110 – Floating Ground EMI, 20 V / 2.25 A Load [Line Scan].



Date: 14.NOV.2019 17:43:14

115 VAC.



Date: 14.NOV.2019 17:45:20

230 VAC.

Figure 111 – Floating Ground EMI, 20 V / 2.25 A Load [Neutral Scan].



17 Combination Wave Surge

The unit was subjected to ± 1000 V differential mode and ± 2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

17.1 Differential Mode Surge (L1 to L2), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+1000	L1 to L2	0	Pass	Pass
-1000	L1 to L2	0	Pass	Pass
+1000	L1 to L2	90	Pass	Pass
-1000	L1 to L2	90	Pass	Pass
+1000	L1 to L2	180	Pass	Pass
-1000	L1 to L2	180	Pass	Pass
+1000	L1 to L2	270	Pass	Pass
-1000	L1 to L2	270	Pass	Pass

17.2 Common Mode Surge (L1 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+2000	L1 to PE	0	Pass	Pass
-2000	L1 to PE	0	Pass	Pass
+2000	L1 to PE	90	Pass	Pass
-2000	L1 to PE	90	Pass	Pass
+2000	L1 to PE	180	Pass	Pass
-2000	L1 to PE	180	Pass	Pass
+2000	L1 to PE	270	Pass	Pass
-2000	L1 to PE	270	Pass	Pass

17.3 Common Mode Surge (L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+2000	L2 to PE	0	Pass	Pass
-2000	L2 to PE	0	Pass	Pass
+2000	L2 to PE	90	Pass	Pass
-2000	L2 to PE	90	Pass	Pass*
+2000	L2 to PE	180	Pass	Pass
-2000	L2 to PE	180	Pass	Pass
+2000	L2 to PE	270	Pass	Pass
-2000	L2 to PE	270	Pass	Pass

17.4 Common Mode Surge (L1, L2 to PE), 230 VAC Input

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 20 V / 0 A (Pass/Fail)	Test Result 20 V / 3 A (Pass/Fail)
+2000	L1, L2 to PE	0	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass
+2000	L1, L2 to PE	180	Pass	Pass
-2000	L1, L2 to PE	180	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass

Pass* - Unit was restarting during some strikes due to line overvoltage protection.

18 Electrostatic Discharge

The unit was tested with ± 8 kV to ± 16.5 kV air discharge and ± 8.8 kV contact discharge at the positive and negative nodes of the output with 10 strikes for each condition.

A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

18.1 Contact Discharge, 230 VAC input

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)	Test Result 20 V / 0 A	Test Result 20 V / 2.25 A
+8.8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8.8	+VOUT	Pass	Pass
	GND	Pass	Pass

18.2 Air Discharge, 230 VAC input

Discharge Voltage (kV)	ESD Strike Location (End of Type-C Cable)	Test Result 20 V / 0 A	Test Result 20 V / 2.25 A
+8	+VOUT	Pass	Pass
	GND	Pass	Pass
-8	+VOUT	Pass	Pass
	GND	Pass	Pass
+10	+VOUT	Pass	Pass
	GND	Pass	Pass
-10	+VOUT	Pass	Pass
	GND	Pass	Pass
+12	+VOUT	Pass	Pass
	GND	Pass	Pass
-12	+VOUT	Pass	Pass
	GND	Pass	Pass
+14	+VOUT	Pass	Pass
	GND	Pass	Pass
-14	+VOUT	Pass	Pass
	GND	Pass	Pass
+16.5	+VOUT	Pass*	Pass*
	GND	Pass	Pass
-16.5	+VOUT	Pass*	Pass*
	GND	Pass	Pass

Pass*- Sometimes unit restarts after the strike.

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
04-Feb-20	SC	1.0	Initial Release.	Apps & Mktg



For the latest updates, visit our website: www.power.com

Reference Designs are technical proposals concerning how to use Power Integrations' gate drivers in particular applications and/or with certain power modules. These proposals are "as is" and are not subject to any qualification process. The suitability, implementation and qualification are the sole responsibility of the end user. The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein. No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits' external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.power.com/ip.htm>.

Power Integrations, the Power Integrations logo, CAPZero, ChiPhy, CHY, DPA-Switch, EcoSmart, E-Shield, eSIP, eSOP, HiperPLC, HiperPFS, HiperTFS, InnoSwitch, Innovation in Power Conversion, InSOP, LinkSwitch, LinkZero, LYTSwitch, SENZero, TinySwitch, TOPSwitch, PI, PI Expert, PowiGaN, SCALE, SCALE-1, SCALE-2, SCALE-3 and SCALE-iDriver, are trademarks of Power Integrations, Inc. Other trademarks are property of their respective companies. ©2019, Power Integrations, Inc.

Power Integrations Worldwide Sales Support Locations**WORLD HEADQUARTERS**

5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

CHINA (SHANGHAI)

Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

CHINA (SHENZHEN)

17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

GERMANY (AC-DC/LED Sales)

Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

GERMANY (Gate Driver Sales)

HellwegForum 1
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

INDIA

#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

ITALY

Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

JAPAN

Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

KOREA

RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

SINGAPORE

51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

TAIWAN

5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK

Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com

