2SP0215F2Q0C
SCALE EV Family

Automotive Dual Channel Plug and Play
Gate Driver for 17 mm IGBT Modules

PRELIMINARY

Product Highlights

- Ready-to-use dual channel gate driver solution with reinforced isolation for 17 mm IGBT power modules up to 1200 V
- Up to 20 kHz switching frequency
- Digital Bitstream diagnostic output
- Single 5 V Supply
- Integrated Dual 2 W DC/DC converters
- Rail-to-Rail stabilized secondary side output voltage
- -40 °C to +85°C operating ambient temperature
- ± 50 kV / µs common-mode transient immunity
- Operation up to 5500 m altitude
- 5 V Input-Logic

Advanced Protection, Safety and Diagnostic Features

- DC-link Active-Discharge (AD) function
- Active Short-Circuit (ASC) function
- Galvanically isolated IGBT module NTC temperature measurement
- Galvanically isolated PCB NTC temperature measurement
- Advanced Resistive Overvoltage Control (AROC)
- Undervoltage monitoring (UVLO) for primary- and Undervoltage warning (UVW) for secondary side
- Secondary side overvoltage monitoring (OVW)
- Gate monitoring
- Input Interlock
- DC/DC controller overcurrent monitoring
- Two stage primary- and secondary side IC temperature monitoring
- Power-Semiconductor short circuit detection (DESAT)
- FluxLink™ signal transfer monitoring
- Active Miller clamp
- Conformally coated
- Technical cleanliness up to 1 mm

Functional Safety Compliance

- Enables up to ASIL D in automotive traction systems
- SEooC according to ISO 26262

Full Safety and Regulatory Compliance

- AEC-Q 100/101/200 components
- IATF 16949 production facilities
- Clearance and creepage distances between primary and secondary sides meet requirements for reinforced isolation (IEC 60664-1, IEC 60664-3)
- 100% production partial discharge test
- 100% production HIPOT testing at 3395 V_{RMS} for 1 s

Applications

- e-Bus and e-Truck traction inverter
- BEV automotive traction inverter
- Diesel electric traction inverter
- Fuel cell inverter
- Agricultural and construction vehicles and equipment
- Other automotive and industrial applications
- General purpose drives

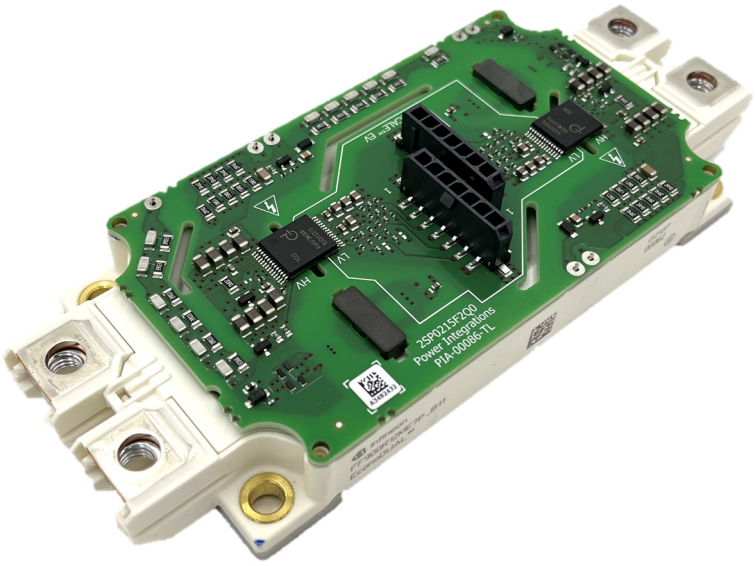


Figure 1. 2SP0215F2Q0C Mounted on Target Power Semiconductor Module.

Product Portfolio

Order Code	Module Technology	Voltage Class	Current Class	Package	IGBT Module Supplier
2SP0215F2Q0C-FF900R12ME7W_B11	Si-IGBT Gen7, Si-Diode	1200 V	900 A	EconoDUAL	Infineon

Table 1 2SP0215F2Q0C Portfolio

Functional Block Diagram

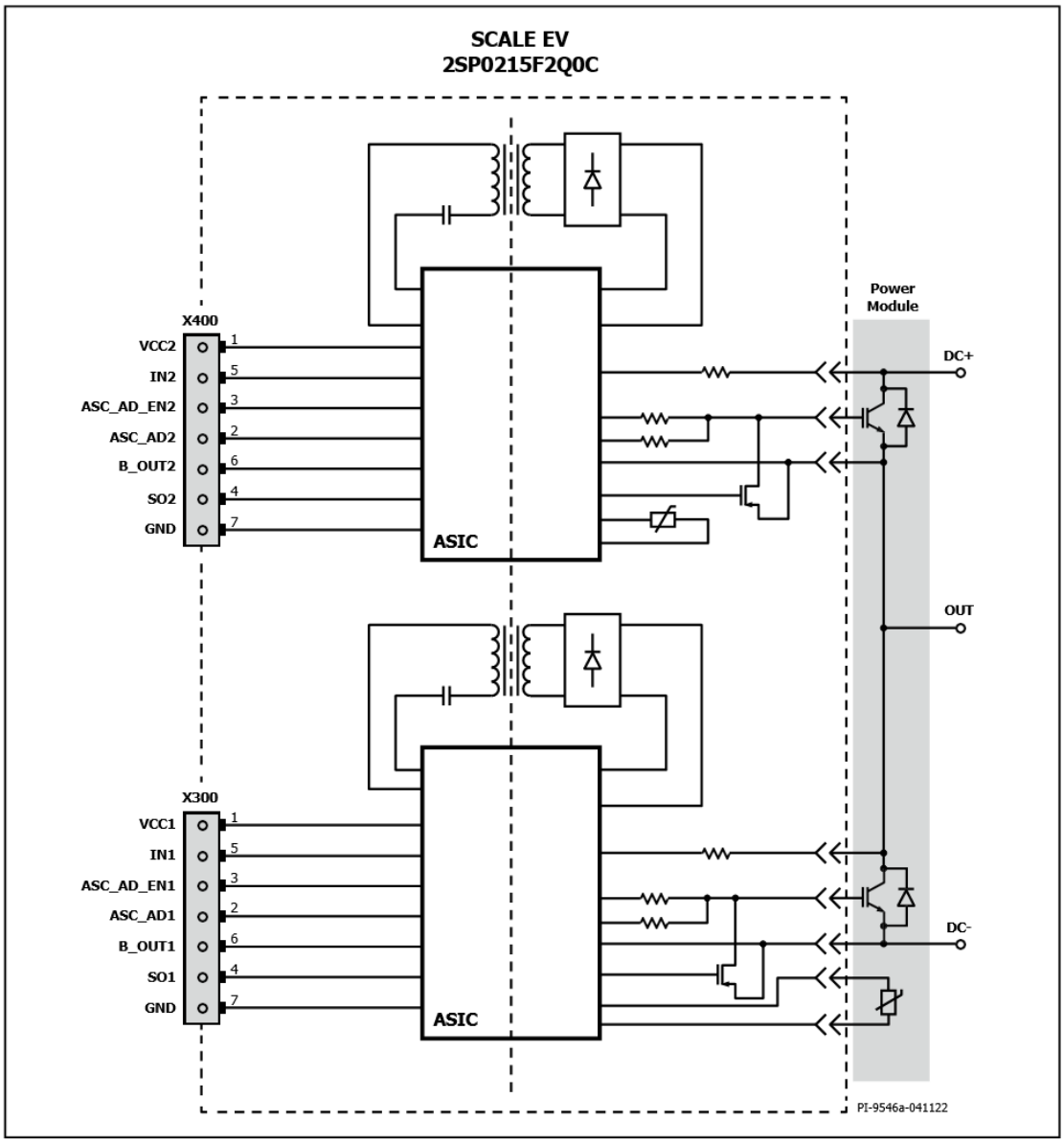


Figure 2. Block Diagram 2SP0215F2Q0C.

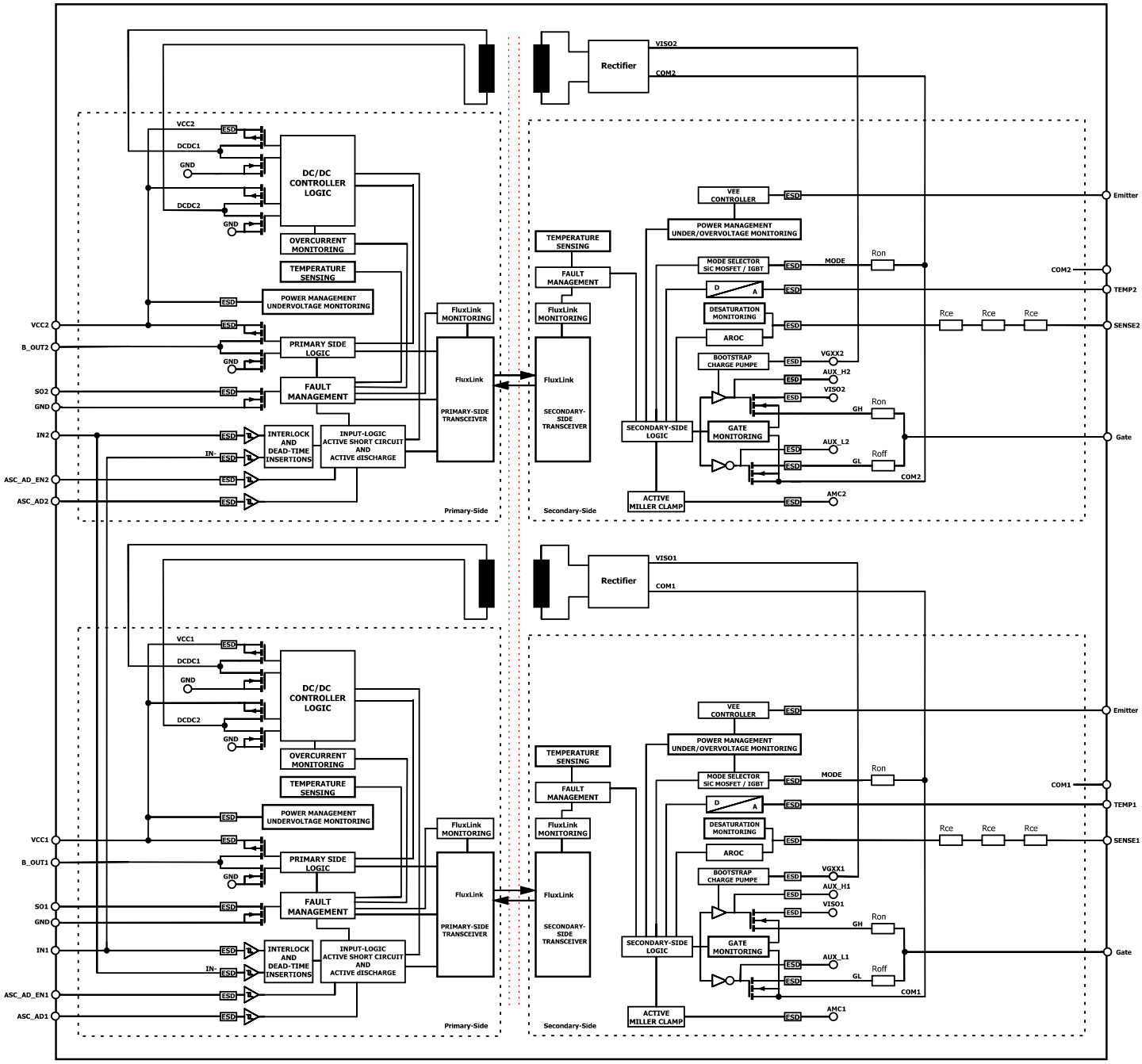


Figure 3. Functional Block Diagram 2SP0215F2Q0C.

Interface Description

Connector X300 (BOT-Channel)

Connection to external system controller from bottom domain (Molex Micro-Fit 3.0 connector).

<VCC1 (Pin 1)>

Primary side 5 V supply voltage.

<ASC_AD1> (Pin 2)

This pin determines together with <ASC_AD_EN> the Active Short Circuit (ASC) and Active Discharge (AD) operating mode.

<ASC_AD_EN1> (Pin 3)

This pin determines together with <ASC_AD> the Active Short Circuit (ASC) and Active Discharge (AD) operating mode.

<SO1> (Pin 4)

Open drain output fault signal active Low.

<IN1> (Pin 5)

Primary side control input signal.

<B_OUT1> (Pin 6)

Bitstream output for diagnostics and NTC temperature value.

<GND> (Pin 7)

Primary side <GND> connection with reference to< VCC1>.

Connector X400 (TOP-Channel)

Connection to external system controller from top domain (Molex Micro-Fit 3.0 connector).

<VCC2> (Pin 1)

Primary side 5 V supply voltage.

<ASC_AD2> (Pin 2)

This pin determines together with <ASC_AD_EN> the Active Short Circuit (ASC) and Active Discharge (AD) operating mode.

<ASC_AD_EN2> (Pin 3)

This pin determines together with <ASC_AD> the Active Short Circuit (ASC) and Active Discharge (AD) operating mode.

<SO2> (Pin 4)

Open drain output fault signal active Low.

<IN2> (Pin 5)

Primary side input logic signal.

<B_OUT2> (Pin 6)

Bitstream output for diagnostics and NTC temperature value.

<GND> (Pin 7)

Primary side <GND> connection with reference to <VCC2>.

Quick Start Guide

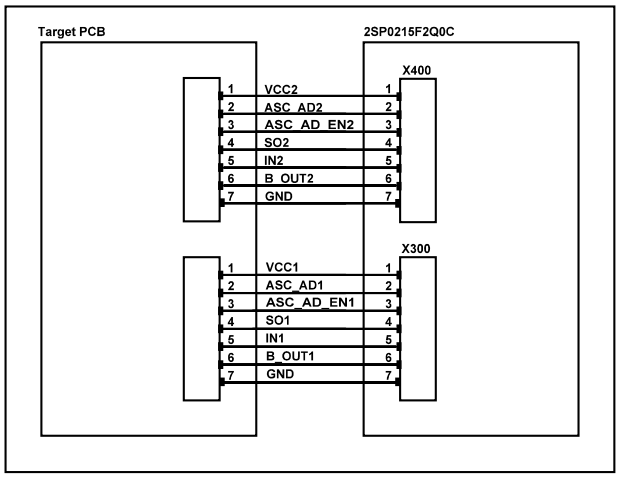


Figure 4. Interface Target System PCB to 2SP0215F2Q0C.

Connector X300

Connection to external system controller from bottom domain (Molex Micro-Fit 3.0 connector).

Connector X400

Connection to external system controller from top domain (Molex Micro-Fit 3.0 connector).

The 2SP0215F2Q0C can be commissioned easily to evaluate the performance in various applications. For this, follow the procedure below:

1. With all power off, connect the target system to Connector X300 and Connector X400.
2. Turn on the power supplies for V_{VCC1} and V_{VCC2}.
3. Apply PWM voltages signals according to Table 2 at the logic input pin <IN1> and <IN2>.

Input Signal	Waveform	V_{LOW}	V_{HIGH}	f_{SW}	Phase
IN1	Rectangular	0 V	5 V	10 kHz	0°
IN2	Rectangular	0 V	5 V	10 kHz	180°

Table 2: Example PWM Signal Conditions

Note 1: The minimum gate driver integrated hardware dead time of >465 ns must be inserted into the PWM signals to avoid dead-time warning.

4. The ASC Mode (Active-Short-Circuit) can be activated by applying logic High to <ASC_AD_EN> either on each BOT- or on each TOP-Channels of an assumed two level 3-Phase inverter. ASC_AD_EN will override the IN1/IN2 signal states.

The following Table 3 shows the possible modes:

ASC_AD_EN	ASC_AD	Mode
0 V	0 V	Normal Mode
5 V	0 V	ASC Mode Gate Output turned-off
5 V	5 V	ASC Mode Gate Output turned-on

Table 3 Active Short-Circuit Mode.

5. The AD (Active Discharge) can be activated by applying logic High to <ASC_AD> while keeping <ASC_AD_EN> at logic Low.

The following Table 4 shows the possible modes:

ASC_AD_EN	ASC_AD	Mode
0 V	0 V	Normal Mode
0 V	5 V	AD Mode

Table 4 Active Discharge Mode.

6. A logic Low signal on <SOx> indicates a major fault. Therefore, the target system must set all IN signals to logic Low to avoid a damage of the power semiconductor chips. <B_OUTx> continuously sends a serial stream of data with detailed information about the actual status, temperature, errors & warnings.

Recommendations

To achieve the optimum performance of the 2SP0215F2Q0C gate driver consider the following in the design of the target system controller PCB..

Inputs VCC1 and VCC2

- <VCC1> and <VCC2> must be supplied from independent power supplies to be compliant with functional safety.
- TOP- and BOT-Channel must have a common GND.
- <VCC1> and <VCC2> must be capable of providing a variable output current of up to 500 mA. Actual value depends on the power semiconductor gate charge and switching frequency.

Inputs ASC_ADx, ASC_AD_ENx and INx

For 3.3 V microcontroller applications, it is recommended to use a level shifter from 3.3 V to 5 V on the target PCB for the inputs <ASC_ADx>, <ASC_AD_ENx> and <INx>. It is recommended to consider the level shifter behavior during power up, power down sequences to avoid unexpected results.

An example for the logic inputs <IN1> and <IN2> is given in Figure 5. The same circuit should be used for all other inputs.

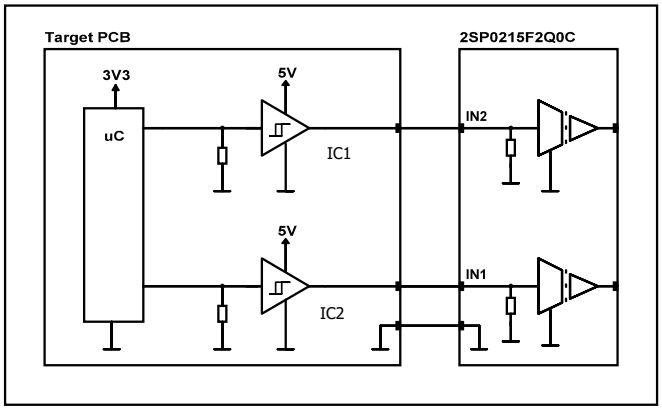


Figure 5. Recommended <INx> Level-Shifter for 3.3 V Microcontroller-Applications.

The following requirements must be considered:

Schmitt Trigger IC1 and IC2

- Use a Schmitt-Trigger with a supply voltage of 5 V
- The Schmitt-Trigger must be compatible with 3.3 V input signals
- The Schmitt-Trigger output must remain logic Low during power up/down conditions

Outputs B_OUTx and SOx

For 3.3 V microcontroller applications, it is recommended to use a level shifter from 5 V to 3.3 V on the target PCB for the output signals <B_OUTx> and <SOx>.

An example for the output SO1 and SO2 is given in Figure 6. The same circuit must be used for all other digital output pins.

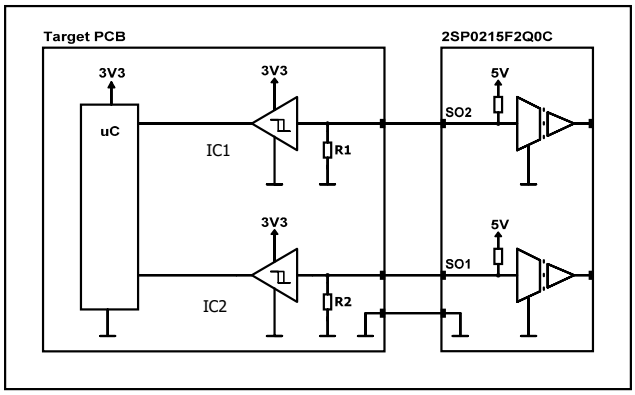


Figure 6. Recommended Level-Shifter for 3.3 V Microcontroller-Applications for <SOx> outputs.

The following requirements must be considered:

Pull-Down Resistors R1 and R2

- Use a weak 100 kΩ pull-down resistor in the target design for detecting interrupted wiring conditions.

Schmitt Trigger IC1 and IC2

- Use a Schmitt-Trigger with a supply voltage of 3.3 V
- The Schmitt-Trigger must be compatible with 5 V input signals
- The Schmitt-Trigger output must remain logic Low during power up/down conditions

General Description

The 2SP0215F2Q0C is an automotive dual channel gate driver for 17 mm EconoDUAL™3 IGBT modules. The plug and play gate driver board is designed for applications which requires automotive qualification like e-Bus, e-Truck, battery electrical vehicles, hybrid electrical vehicles, or fuel cell inverters operating with system voltages up to 1000 V.. Additionally, the plug and play gate driver can control industrial IGBT modules in industrial applications. The 2SP0215F2Q0C is offered in different variants, optimized to meet the requirements of a specific IGBT module.

Primary Side

- Integrated LLC DC/DC power supply
- Interlocking
- Active-Short-Circuit (ASC) function
- DC Link Active-Discharge (AD) function
- Failure output (low latency)
- Digital Bitstream diagnostic output
- IGBT module and PCB temperature output

Secondary Side

- Regulated secondary side power supply
- Galvanically isolated IGBT module NTC readout
- Galvanically isolated PCB NTC readout
- Active Miller clamping

Diagnostic and Monitoring

- Under- and over-voltage monitoring and warning
- Gate monitoring
- FluxLink™ communication monitoring
- Communication parity check
- Primary side DC/DC overcurrent monitoring
- Primary side DC/DC two level over-temperature monitoring
- Gate driver output stage overtemperature monitoring
- Short pulse diagnostic

Protection

- Minimum dead time
- PWM input signal interlocking
- Advanced resistive overvoltage control (AROC)
- Short-Circuit

In the following section, all functions and features are briefly described. A more detailed description can be found in in chapter Functional Description .

Primary Side Power Supply

Two individual supply voltages V_{VCC2} to GND (TOP-Channel) and V_{VCC1} to GND (BOT-Channel) respectively are necessary to operate the 2SP0215F2Q0C.

Safe Power-Up and Power-Down

It is required that during the power-up and the power-down events, <INx> pins remains logic Low. Any supply voltage related to V_{VCC} and GND must be stabilized by capacitors. After the supply voltages reach their recommended nominal values, the gate driver will start to operate after a time delay t_{START}.

Integrated DC/DC Converter

Each gate driver channel offers a galvanically isolated DC/DC controller, power stage, transformer and rectifier which supplies the secondary side.

Input Gate Control Signals

The input <IN1> (BOT-Channel) and <IN2> (TOP-Channel) logic is designed to operate with controllers using 5 V CMOS logic. The gate control signals will be transferred, via galvanic isolation, to the secondary side, defining the on/off state of the power semiconductor chips.

Input Logic Interlocking

The input logic signals IN1 and IN2 are interlocked to each other. This feature prevents an accidently turn-on for both channels at the same time.

Note: This function is deliberately disabled if Active Discharge (AD) is enabled

Active-Short-Circuit (ASC) Function

For functional safety requirements and overvoltage protection of the high voltage system, the 2SP0215F2Q0C provides an Active-Short-Circuit (ASC) mode, which by system request enables a short circuit to be created across the motor terminals.

DC Link Active Discharge (AD) Function

For functional safety requirements the 2SP0215F2Q0C provides an Active Discharge (AD) mode. Once activated, this mode will discharge the DC-Link capacitor by using the IGBT module. This provides cost and board area savings compared to a discrete external circuit.

Temperature Measurement

The 2SP0215F2Q0C provides two galvanically isolated NTC readouts for the BOT/TOP-Channel. One for the power semiconductor and one for the PCB.

Active Miller Clamp

Active Miller clamp can prevent unexpected turn on situations due to unwanted switching of the complementary power semiconductor in a half bridge configuration. The 2SP0215F2Q0C active Miller clamp function is turned on after the corresponding power semiconductor chip is turned off and the gate voltage is below a certain threshold.

Gate Driver Output Stage

The 2SP0215F2Q0C contains a high current n-channel push-pull driver stage, compatible with the the large gate charges of high current IGBT modules.

Under and Overvoltage Monitoring and Warning

Each gate driver channel continuously monitors the supply voltage V_{VCC}. If the supply voltage drops below a specific value, the affected channel will enter the UVLO-Mode and indicates the condition with a static logic Low on <SOx> and logic High on <B_OUTx>.

Additionally, each channel continuously monitors the secondary side supply voltage. In case of over- and undervoltage conditions, the corresponding warning Bits in the Bitstream output are asserted.

Gate Failure Monitoring

The 2SP0215F2Q0C compares continuously the gate voltage of each channel with the desired state given by <IN1>/<IN2>. In case of an unexpected condition, the corresponding warning Bit in the Bitstream output is asserted.

FluxLink™ Communication Monitoring

The 2SP0215F2Q0C continuously monitors the status of the communication (FluxLink™) between the primary side and secondary side for both channels. In case of an unexpected condition, the corresponding warning Bit in the Bitstream output is asserted.

Communication Parity Check

The secondary side sends continuously status information to the primary side. For safety reasons the secondary side inserts a parity Bit in each data frame to provide a way to detect corrupted data by the target system.

Note: The parity Bit covers secondary side data only.

Secondary Side Overtemperature Monitoring

The gate driver 2SP0215F2Q0C monitors continuously the secondary side power semiconductor temperature for each channel. In case of an overtemperature, the corresponding warning Bit in the Bitstream output is asserted.

Hardware Dead Time

To prevent half bridge shoot through events, the 2SP0215F2Q0C ensures a minimum dead time, if the target system dead time is below a specific value then a minimum deadtime is inserted and a warning bit in the bitstream output is asserted..

Advanced Resistive Overvoltage Control (AROC)

If the gate driver is in a turn-off transition or in off-state, the AROC overvoltage limitation algorithm is activated. This provides a deterministic maximum collector voltage regardless of collector current including turn-off after a short circuit event.

Short-Circuit Protection

When the gate driver is in a turn-on transition or in the on-state, the short-circuit detection algorithm is activated after the delay time $t_{SENSE(BL)}$ has elapsed.

FluxLink™ Technology

The FluxLink™ technology allows signals to be transmitted across a reinforced isolation barrier without the need for magnetic materials. By providing >0.4 mm spacing through solid insulation the reinforced isolation barrier is physically rugged. FluxLink™ provides bidirectional communication between primary- and secondary side.

Short Pulse Protection

The 2SP0215F2Q0C continuously monitors <IN1>/<IN2>. Pulse durations lower than a specified value will be extended and the corresponding warning Bit in the Bitstream output is asserted.

Note: A minimum turn-on time for IGBTs and diodes is necessary to avoid diode snappiness especially at low temperatures. Therefore, it is recommended that PWM software include a minimum on time larger than the gate driver minimum hardware on time.

Functional Description

A detailed explanation of function and features is provided below.

Primary Side Power Supply

Two individual supply voltages V_{VCC2} to GND (TOP-Channel) and V_{VCC1} to GND (BOT-Channel) are necessary to operate the 2SP0215F2Q0C. Current consumption in non-Switching operation is provided in the "electrical data" section. Depending on the specific IGBT module, switching frequency and temperature the active current consumption varies.

Note 1: For greater functional safety, it is recommended to use two independent power supplies for V_{VCC1} and V_{VCC2} The primary GND is common for V_{VCC1} and V_{VCC2}.

Note 2: The gate driver does not provide reverse voltage protection

Note 3: The wiring between the target system and X400 and X300 connectors must be as short as possible. Touching or crossing high voltage potentials is not permitted.

Integrated DC/DC Converter

To generate isolated voltages to drive the gates of the power devices the 2SP0215F2Q0C contains an integrated DC/DC controller, power stage MOSFETs and transformer for each channel.

The 2SP0215F2Q0C monitors the die temperatures related to the DC/DC converter output stage and current on the primary side for each channel.

An overview of the different sensor signals and the corresponding reactions is provided in Table 1 below. A distinction is made between the following sensor signals:

- The temperature threshold $OT1_{DCDC}$ (overtemperature warning level 1)
- The temperature threshold $OT2_{DCDC}$ (overtemperature warning level 2)
- Over current I_{DCDC1} and/or I_{DCDC2}

Table 5 gives an overview of the behavior of the DC/DC controllers during the start-up phase and in normal operation . An "X" indicates that the respective threshold value of the sensor signal has been reached. The "B_OUT" column lists the Bits that are set to logic Low in the presence of an error/warning. For example: during startup, detection of over current will cause the DC/DC controller to stop. However once in stable operation the controller will continue to operate but in both cases B_OUT[25] bit will be asserted to indicate a warning condition.

Die Temperature Threshold $OT1_{DCDC}$	Die Temperature Threshold $OT2_{DCDC}$	Over Current I_{DCDC1} and/or I_{DCDC2}	<B_OUTx>	DC/DC Controller Operation Start-up Phase	DC/DC Controller Operation Stable Operation
-	-	-	-	Normal Operation	Normal Operation
X	-	-	B_OUT[23]	Normal Operation	Normal Operation
-	X	-	B_OUT[23] B_OUT[24]	Turned-Off	Turned-Off
-	-	X	B_OUT[25]	Turned-Off	Normal Operation
X	-	X	B_OUT[23] B_OUT[25]	Turned-Off	Normal Operation
-	X	X	B_OUT[23] B_OUT[24] B_OUT[25]	Turned-Off	Turned-Off

Table 5 DC/DC Controller States at Different Conditions for Each Channel

Safe Power-Up and Power-Down

It is required that during the power-up and the power-down events, <INx> as well as <ASC_ADx> and <ASC_AD_ENx> inputs remains at logic Low. Any supply voltage related to V_{VCCx} and GND must be well stabilized. If the supply voltages reach their nominal values, the gate driver will start to operate after a delay time t_{START}.

Input Logic Interlocking

The input logic signals <IN1> and <IN2> are interlocked from each other. This feature prevents turn-on of both channels at the same time.

An IGBT half-bridge short-circuit is safely prevented in standard operation conditions. If an interlock event occurs, B_OUT [28] of both channels will be set to logic Low and both gate driver output stages will be turned-off.

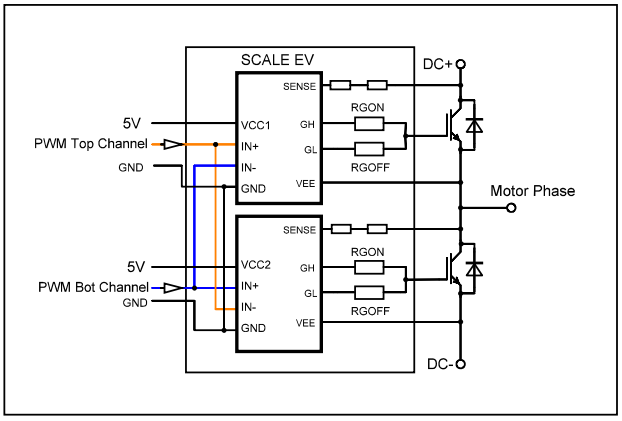


Figure 7. Interlocking Function in Half-Bridge Configuration.

Note 1: If the Active Discharge Function is enabled for a channel, the Interlocking-Function of the same channel is disabled.

Motor Active Short-Circuit Mode (ASC)

For functional safety and protection of the inverter from excessive voltage, the 2SP0215F2Q0C provides an Active-Short-Circuit (ASC) mode which, by system request, applies a short circuit across the motor terminals.

ASC mode allows the system to keep the gate driver output stage in a defined state either permanently turned-on or permanently turned-off, regardless of <INx> state. This feature makes it possible to short the motor terminals to create a negative torque, decelerating the vehicle in a controlled manner.

The ASC Mode can be activated according the following Table 6

ASC_AD_EN	ASC_AD	Mode
0 V	0 V	Normal Mode
5 V	0 V	ASC Mode Gate Output turned-off
5 V	5 V	ASC Mode Gate Output turned-on

Table 6 Active Short-Circuit Mode.

DC Link Active Discharge (AD) Function

To avoid the need for additional components for discharging the DC-Link capacitance, the 2SP0215F2Q0C provides an Active Discharge (AD) mode. The principle of the AD mode is to discharge the DC-Link energy through the IGBT module of one or more half-bridges. The IGBT modules are operated in their linear region (reduced gate voltage) and pulsed at a low duty cycle. Linear operation allows the IGBT module acts as a current limiting device.

The AD mode is initiated by applying logic High at pin <ASC_AD> while keeping <ASC_AD_EN> at logic Low.

ASC_AD_EN	ASC_AD	Mode
0 V	0 V	Normal Mode
0 V	5 V	AD Mode

Table 7 Active Discharge Mode

To discharge a DC-Link capacitor the scheme of Figure 9 must be followed. In Figure 8 an implementation example of the AD function in a target system is shown.

Note 1: First the gate drivers from both channels must be operating in normal mode; the secondary side voltages have reached steady state.

Note 2: In AD mode, the input logic interlocking is ignored.

Timing & Details

After setting the <ASC_AD_EN> and <ASC_AD> signals the gate drivers reduce the secondary side supply voltages and the 2SP0215F2Q sends an undervoltage warning on both channels. Subsequently the target system must provide logic High pulses with limited duration ≤ $t_{SENSE(BL)}$ to <IN1> and <IN2> simultaneously.

After discharging the DC-Link, the normal mode can be restored by setting the <ASC_AD> to logic Low. The gate drivers restore the secondary side supply voltages, and the gate drivers resume normal operation.

Note 2: If $t_{SENSE(BL)}$ is exceeded the short circuit protection can be activated unexpectedly. This also functions as a safety mechanism, preventing excessive power device dissipation should the system uC command a high duty cycle.

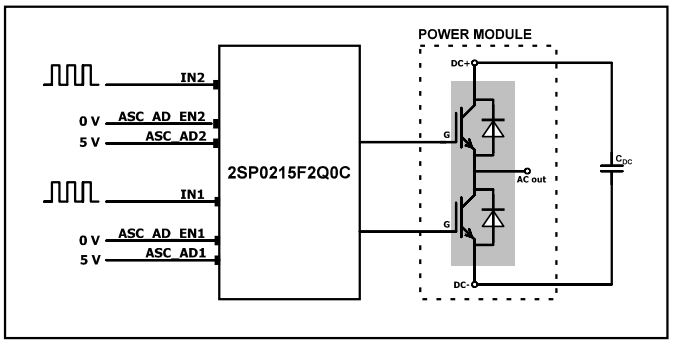


Figure 8. Active Discharge Implementation.

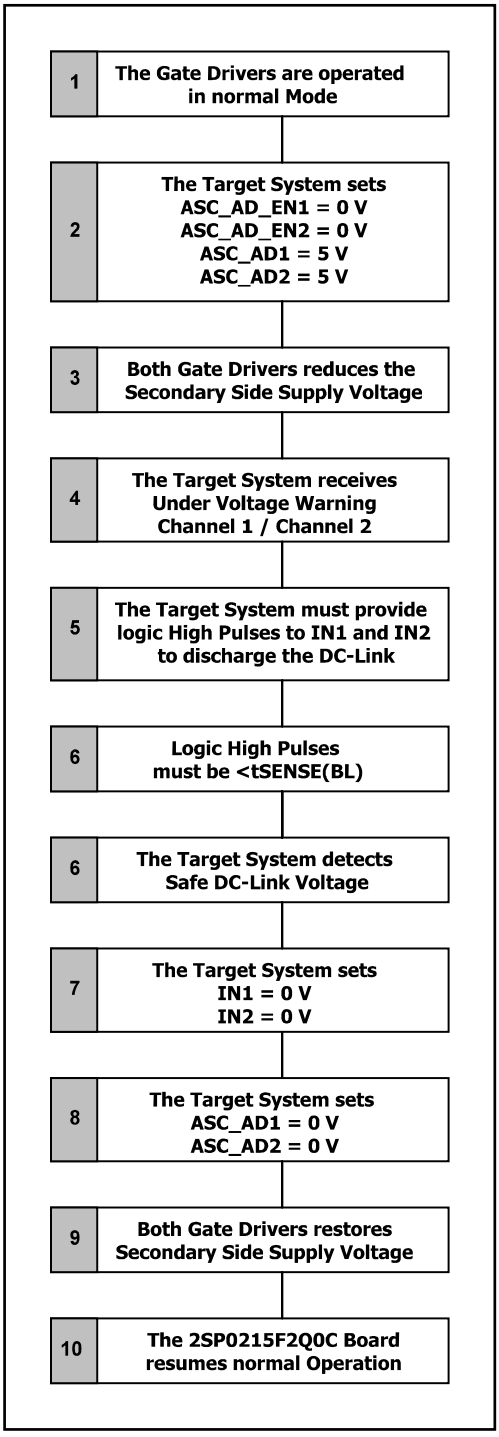


Figure 9. Active Discharge Scheme.

Example:

The simulation results in 8 and Figure 10 show that the discharge of an 1100 uFmF capacitor, charged at 850 V can be achieved in < 1s by using pulses of 2 µs length and 1 kHz repetition rate. The temperature rise of the IGBT devices of <5 Kelvin provides a suitable margin even at 125°C baseplate temperature.

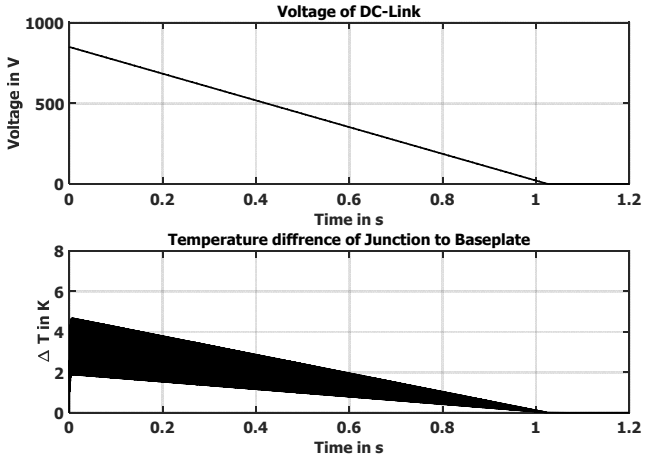


Figure 10. Thermal Simulation of active discharge using FF900R12ME7W_B11 with 1100 µF Cap at 850 V, 2 µs, 1 kHz.

Capacitance	1100 µF
DC-Link Voltage	850 V
PWM Switching Frequency	1 kHz
Pulse width	2 µs
Discharge Time	< 2 s
ΔT in K	5 K

Table 8 Simulation Results Active Discharge Mode.

Note: It is highly recommended to evaluate the real thermal behavior in the final application which might differ from the example. In case of thermal overstressing, the pulse repetition rate can be reduced.

Secondary Side Power Supply

The secondary side supply voltage (V_{VISO} vs. COM) is a unipolar voltage generated from the primary side via a galvanically isolated DC/DC transformer. The positive gate-emitter voltage is provided by V_{VISO} with respect to V_{VEE} and the negative gate-emitter voltage by COM with respect to V_{VEE}. An integrated regulator keeps V_{VISO} to V_{VEE} stable.

NTC Temperature Measurement

The 2SP0215F2Q0C provides a galvanically isolated NTC readout. The bottom channel is designed to read the IGBT module integrated NTC resistor. The TOP-Channel is designed to read the SMD NTC placed on the PCB, position is shown in Figure 11.

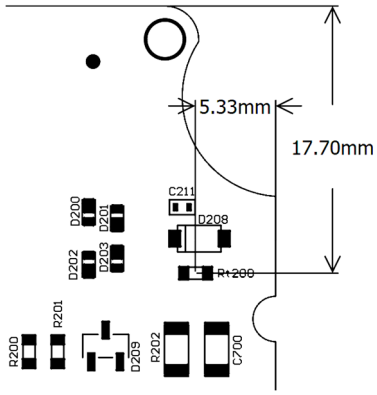


Figure 11. SMD Thermistor for TOP Channel Mounted on PCB

The NTC resistance is digitized by a 12-Bit analog to digital converter (ADC) before it is transferred to B_OUT.

Equation 1 describes the function R(B_OUT[2_{MSB}:13_{LSB}]) by applying the following formula:

$$\boldsymbol{R}_{B\_OUT} = 32 \times \frac{\boldsymbol{V}_{TEMP}}{\boldsymbol{I}_{TEMP} \times B_{OUT}[2:13]} \qquad \text{Eq. 1}$$

Example:

For B_OUT [2:13] = 011011100010_2 the following resistance value can be calculated:

$$\boldsymbol{R}_{B\_out} = 32 \times \frac{0.3\ V}{20\ \mu A \times 1762} = 272\ \Omega$$

The following Figure 12 shows the PCB temperature in accordance to B_OUT[2:13]:

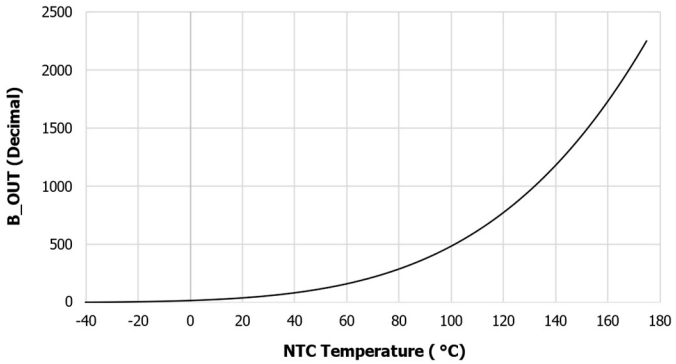


Figure 12. B_OUT Decimal Temperature Value as a function of Board NTC Temperature

The following Figure 13 shows the IGBT NTC temperature in accordance to B_OUT[2:13]:

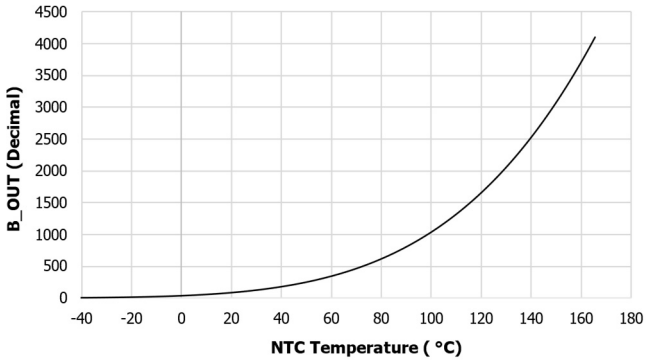


Figure 13. B_OUT Decimal Temperature Value as a function of IGBT Module NTC Temperature

Integrated Active Miller Clamp

To avoid parasitic turn-on effects in half-bridge topologies and during switching events of other power semiconductor chips, the active Miller clamp provides a low impedance connection between the gate of the power semiconductor and the negative supply voltage. Charge injected by switching dv/dt via the Miller capacitance is shorted to the negative gate voltage, keeping the gate safely below the device threshold voltage.

Hardware Dead Time

To prevent half-bridge short circuits, the 2SP0215F2Q0C ensures a minimum dead time, if the target system dead time insertion is below a specific value.

In case that the dead-time between <IN1> and <IN2> is smaller than t_{DT}, the gate driver will insert a minimum dead time of t_{DT} and set B_OUT [28] to logic low for indication.

Note 1: It is recommended to ensure a suitable dead time in the target system.

Note 2: It is recommended to set up the PWM software with a minimum on time for IGBTs. Short duration pulses can damage the IGBT or diode because of high di/dt and dv/dt.

<SOx> and <B_OUTx> Failure and Diagnostics

The gate driver uses two logic output pins <SOx> and <B_OUTx> per channel to support failure management and diagnostics.

<SOx> is an open drain fast-responding fault indicator. A logic low indicates a fault state, and the corresponding power semiconductor will be turned off by the gate driver. The gate driver will remain in this state until the next logic low-high transition of the corresponding channel input INx occurs. If SO is recognized as logic Low, it is recommended to switch off all channels immediately.

Note 1: Secondary side failure generates a logic low pulse of minimum t_{so} at <SOx>. The gate driver will remain in this state until the next logic low-high transition of the corresponding channel input INx occurs after this blanking time of t_{so}.

Note 2: A primary side UVLO-Failure generates a continuously logic low SO if the upper threshold of the UVLO is not exceeded. While this fault condition remains, the power semiconductor will be kept switched off. The gate driver will remain in this state until the UVLO is exceeded and the next logic low-high transition of the corresponding channel input INx occurs.

Note 3: Whenever a SO is asserted (active Low) the next BitStream data packet contains just zeroes. The subsequent data packet will reflect valid information including the cause for the fault to be asserted.

B_OUT is a digital Bitstream output (Figure 14). Multiple different status conditions can be determined by using <SO> and< B_OUT> together.

Details are shown in Table 9:

SOx	B_OUTx[]	Fault / Warning
Low	High	V_{VCCx} undervoltage fault
High	[14] = Low	V_{VISO} undervoltage warning UVW_{VISO}
High	[15] = Low	V_{VISO} overvoltage warning OVW_{VISO}
High	[16] = Low	Gate monitoring warning
High	[17] = Low	Overtemperature warning $OT2_{GD}$
High	[18] = Low	Overtemperature warning $OT1_{GD}$
High	[19] = Low	Secondary side FluxLink™ out of service warning
Low	[19] = Low	Secondary side FluxLink™ out of service fault
Low	[20] = Low	Short-Circuit detection
High	[21] = Low or High	Parity Bit, set in a way that the sum of B_OUT[2:21] high Bits is odd
High	[22] = High	Primary side FluxLink™ out of service warning
High	[23] = High	Overtemperature warning $OT1_{DCDC}$
High	[24] = High	Overtemperature warning $OT2_{DCDC}$
High	[25] = High	Primary side DC/DC Controller overcurrent warning during startup
High	[25] = High	Primary side DC/DC Controller overcurrent warning after startup
High	[27] = High	Dead-Time insertion warning
High	[28] = High	Interlock warning

Table 9 Combined Fault and Status Feedback of SO and B_OUT.

Note: The definition of a logic Low or high condition of <B_OUTx> Bits are determined by the pulse width as defined in Figure 14.

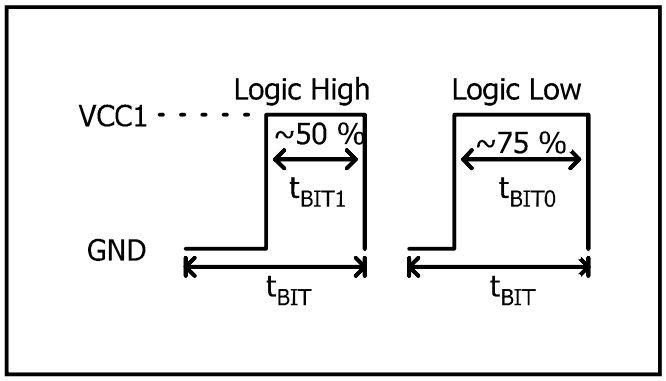


Figure 14. Definition of Logic Low and Logic High Levels at B_OUT

The information of the digital Bitstream B_OUT consists of a start Bit logic High, 27 payload Bits and 1 stop Bit. Prior the start Bit a series of logic Low Bits (B_OUT [idle]) are sent. The number of idle Bits is not fixed. It is defined by the asynchronous frame time $t_{B\,OUT}$ minus the time required for the transmission of the start Bit, Pay Load Bit and the stop Bit.

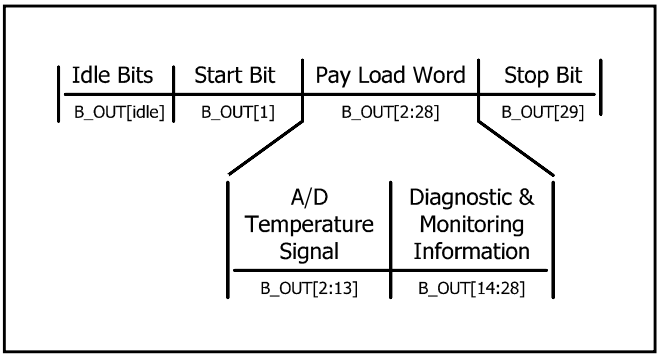


Figure 15. B_OUT Bit Assignment.

The individual faults, warnings and feedbacks listed in Table 9 will be explained below.

Under and Overvoltage Monitoring and Warning

The supply voltages are monitored. In case of an under voltage lock out (UVLO) or over voltage Warning (OVW) a failure or a warning signal is generated.

The undervoltage monitoring function can detect:

- If V_{VCC} (primary side) reaches the undervoltage lockout level $UVLO_{VCCx}$ / $UVLO_{VCC2}$ the related gate driver channel turns-off. <SOx> signal will be set to logic low and <B_OUTx> will remain logic High.
- If V_{VISO} (secondary side) reaches the undervoltage warning level UVW_{VISO1} / UVW_{VISO2}, the related gate driver channel remains active, only a warning is displayed at B_OUT[14] (logic Low).
- If V_{VISO} (secondary side) reaches the overvoltage warning level OVW_{VISO1} / OVW_{VISO2}, the related gate driver channel remains active, only a warning is displayed at B_OUT[15] (logic Low)

Gate Monitoring Failure Diagnostic

The 2SP0215F2Q0C monitors the gate output on the secondary side of each gate driver channel, comparing the expected level with the control input <IN1/2>.

If logic High is applied at <IN1> or <IN2>, the corresponding gate output will turn-on. The output voltage of the gate is measured after the time $t_{GM(ON)}$ has elapsed. The V_{GE} voltage level must be larger than the internal reference value $V_{GM(ON)}$. If not, a gate monitoring warning will be generated by activating the warning Bit B_OUT[16].

Similarly, if logic Low is applied at <IN1/2>, the gate output will turn-off the gate of the power semiconductor chip. The output voltage of the gate is measured after the internal time $t_{GM(OFF)}$ has elapsed. If the voltage level is still higher than the internal reference voltage $V_{GM(OFF)}$, a gate monitoring warning will be generated by activating the warning Bit B_OUT[16].

The gate monitoring function can detect following failures:

- A high resistive gate resistor
- A gate driver communication failure.
- Failed booster stage
- Gate-emitter shorts of the driven power semiconductor chip

Note 1: The digital Bitstream might have a different frequency than the applied command signals at <IN1> or <IN2>. Nevertheless, all switching events will be monitored and any faulty signal reported i.e., a fault condition is latched and reported at the next Bitstream transmission.

FluxLink™ Communication Monitoring

The 2SP0215F2Q0C constantly monitors the status of the internal communication channel (FluxLink™) between the primary and secondary sides for both channels.

The FluxLink™ Communication monitoring function can detect:

- If the communication on the primary side is disturbed for typically 10 µs and no valid message is detected, the gate driver triggers a primary side FluxLink™ out-of-service warning and sets Bit B_OUT [22] to logic Low.
- If the communication on the secondary side is disturbed for typically 10 µs and no valid message is detected, the gate driver triggers a secondary side FluxLink™ out-of-service warning and sets the Bit B_OUT [19] to logic Low.

If the communication fault on the secondary side lasts longer than typically 20 µs, a secondary side FluxLink™-out-of-service fault is triggered, and the SO is set to logic Low for t_{SO} after a delay of $tSO(DL)$ has been elapsed. The related gate driver channel turns-off and remains in a latched condition as long as FluxLink returns to normal operation followed by a transition from logic Low to High on INx.

Communication Parity Check

An additional parity Bit is added to the data which send from secondary side to the primary side. The parity Bit is set at position B_OUT [21] as shown in Figure 16.

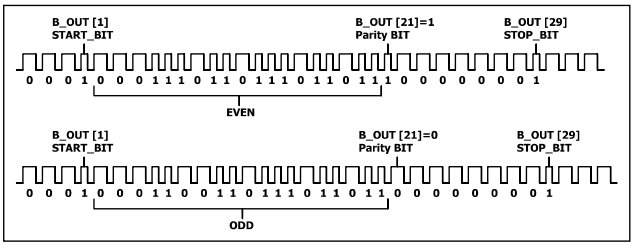


Figure 16. Example for the appended Parity Bit.

The parity Bit is calculated in a way that the sum of logical high Bits [2:21] will be odd.

Gate Driver Output Stage Over-Temperature Monitoring

The temperature of each gate driver channel is monitored on the primary- and secondary side. On the primary side the DC/DC converter output stage and on the secondary side the temperature of the gate driver output stage are monitored.

The overtemperature monitoring function can detect:

- If the temperature on the secondary side exceeds the $OT1_{GD}$ threshold level a warning is issued. The related gate driver channel remains on, only a warning is displayed at B_OUT [18] (logic Low).
- If the temperature further increases reaching $OT2_{GD}$, a second warning is issued. The related gate driver channel also remains on, only a warning is displayed at B_OUT [17] (logic Low).
- If the temperature on the primary side reaches the $OT1_{DCDC}$ threshold level a warning is issued. The related gate driver channel remains on, only a warning is displayed at B_OUT [23] (logic High).
- If the temperature further increases and reaches $OT2_{DCDC}$, a second warning is issued. The related gate driver channel also remains on, only a warning is displayed at B_OUT [24] (Logic High).

Note: The gate driver will not stop its operation. Therefore, to prevent any thermal damage to the gate driver, the target system must initiate suitable action to keep the gate driver operating conditions within its recommended levels.

Advanced Resistive Overvoltage Control (AROC)

AROC is an advanced circuit to limit the V_{CE} overvoltage during IGBT turn-off. If the gate driver is in a turn-off transition or in off-state, the overvoltage limitation algorithm is activated. Control is triggered by a current I_{SENSE} which is derived from the Collector-Emitter-Voltage limited by a resistor and fed into the gate driver IC. If the AROC function is triggered (seen in Figure 17). The gate driver will regulate the gate current to limit the turn-off di/dt and therefore the collector emitter voltage.

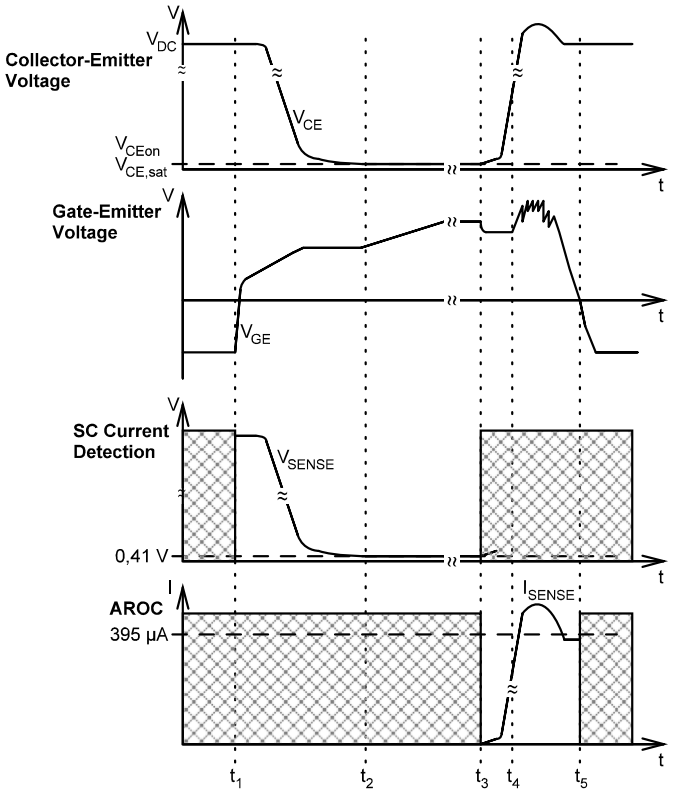


Figure 17. AROC and Short-Circuit Detection on SENSE Potential.

Short-Circuit Protection

When the gate driver is in a turn-on transition or in the on-state, the short-circuit detection is activated after an internal response time $t_{SENSE(BL)}$ has elapsed. A short-circuit condition is detected when the V_{CE} voltage across the collector-emitter of connected power semiconductor chip reaches its set threshold value $V_{SC(TH)}$ and the gate driver responds by turning-off the related gate driver channel. In case of a short circuit event, <SOx> signal transits to logic Low for t_{SO} after a delay of $t_{SO(DL)}$ has been elapsed. Additionally B_OUT[20] is set to logic Low.

Functional Safety

The 2SP0215F2Q0C is designed according to the ISO 26262. The gate driver is intended for the usage in automotive safety applications up to ASIL D. The functional safety aspects are described in the 2SP0215F2Q0C functional safety manual.

The 2SP0215F2Q0C contains two gate driver ICs from Power Integrations.

2SP0215F2Q0C is equipped with various warning and fault functions:

- Warnings are defined such, that the 2SP0215F2Q0C will report the event to the system through the Bitstream but will not activate the <SOx> failure output.
- Faults are defined such, that the 2SP0215F2Q0C will report the event to the system through the Bitstream and in addition <SOx> will be activated.

The warnings and faults can further be subdivided into self-diagnostics and support-to-system diagnostics. The system diagnostics are designed to enhance the system's diagnostic features and thus support the system designer to reach the required level of functional safety.

To satisfy the requirements of a safety related system, 2SP0215F2Q0C offers a variety of safety related features. These features can be integrated into a safety concept from the perspective of a **safety element out of context (SEooC)**:

- Gate Monitoring
- Active Discharge
- Active Short-Circuit
- Galvanically isolated temperature measurement of the IGBT Module NTC
- Galvanically isolated temperature measurement of PCB NTC
- FluxLink control
- Short-circuit detection
- Active Miller Clamp
- DC/DC Die-temperature-measurement
- Undervoltage-Lockout (UVLO) on low voltage side and UVW on high voltage side
- Overvoltage-Warning on high voltage side (OVW)
- Deadtime and Interlock
- Reinforced Insulation
- Diagnostic output (Bitstream), two separate channels

Primary Side Faults	
Under voltage per channel 1/2	The <SOx> output is activated, and a turn-off command is sent to the secondary side (high voltage side) of 2SP0215F2Q0C. For as long as the condition persists B_OUTx is disabled and the 2SP0215F2Q0C does not accept any further commands.

Table 10 Primary Side Fault Diagnostic.

Secondary Side Faults	
Short-circuit monitoring per channel 1/2	Detects if the driven IGBT module goes into short-circuit during turn-on. This is a half-bridge relevant diagnostic and detects if the power switch of the other half of the bridge is turned on or in short-circuit.
Secondary side FluxLink™ out ofservice fault per channel 1/2	Triggered on a timeout if no message is detected after 20 µs. Sends SO command to primary-side and a turn-off command to gate driver output stage.

Table 11 Secondary Side Fault Diagnostic

Primary Side Warnings	
DC/DC over current per channel 1 and 2	Detects DC/DC converter current on the 2SP0215F2Q0C. Activated if current load of DC/DC converter rises over internal threshold $I_{DCDC1,th}$ and/or $I_{DCDC2,th}$.
Violation of IN1/IN2 Interlock	Detects the condition that both <IN1> and <IN2> are high at the same time
Violation of IN1/IN2 dead time	This is a half-bridge relevant warning. An adequate dead- time is also added to avoid that the half-bridge is short circuited. Detects if the dead-time between switching a gate driver respects or not a delay with respect to the gate driver on the other half of the bridge.
Primary side FluxLink™-out-of-service warning	Triggered on a timeout if no valid message is detected after 10 µs.
DC/DC over-temperature level 1	Activated if temperature of DC/DC converter rises over $OT1_{DCDC}$.
DC/DC over-temperature level 2	Activated if temperature of DC/DC converter rises over $OT2_{DCDC}$. The DC/DC converter also turns off as long as the condition persists.

Table 12 Primary Side Diagnostic Warnings.

Secondary Side Warnings	
Undervoltage warningper channel 1 and 2	Activated if secondary side supply voltage goes below internal threshold UVW_{VISO}.
Overvoltage warning per channel 1 and 2	Activated if secondary side supply voltage goes above internal threshold OVW_{VISO}.
Secondary side FluxLink™-out-of-service warning per channel 1 and 2	Triggered on a timeout if no valid message is detected after 10 µs.
Gate monitoring per channel 1 and 2	Reads back gate status and compares to command received on secondary side. If the value is not correct then it latches a warning which will be sent to the primary. Although the warning update is f_{SW}-times slower than the 2SP0215F2Q0C switching frequency f_{SW}, any error is latched and transmitted in the next frame.
Gate driver output stage temperature level 1 per channel 1 and 2	Activated if temperature of gate driver output stage rises over $OT1_{GD}$
Gate driver output stage temperature level 2 per channel 1 and 2	Activated if temperature of gate driver output stage rises over $OT2_{GD}$
CRC parity Bit per channel 1 and 2	An even parity Bit is added to digital Bit stream from secondary- to primary side. It is added to <B_OUTx.>

Table 13 Secondary Side Diagnostic Warnings

Minimum/Maximum Ratings

Parameter	Symbol	Conditions T_A = -40°C to 85°C	Min	Max	Units
Absolute Minimum/Maximum Ratings[1]					
Primary Side Supply Voltage	V_{VCC_x}	Referenced to GND	-0.5	6	V
Logic Input Voltage (Command Signal)[2]	V_{INx}	Referenced to GND	-0.5	V_{VCCx} +0.5	V
Logic Input Voltage ASC_AD_ENx and ASC_ADx	V_{ASCx}	Referenced to GND	-0.5	V_{VCCx} +0.5	V
Logic Output Voltage SOx (Status Signal)	V_{SOx}	Referenced to GND	-0.5	V_{VCCx} +0.5	V
Logic Output Voltage B_OUTx (Bitstream Signal)	V_{B_OUTx}	Referenced to GND	-0.5	V_{VCCx} +0.5	V
Output Current SOx (Status Signal)	I_{SOx}	Open drain sink, 1.5 kOhm internal pull up		3.5	mA
Logic output Current B_OUTx (Bitstream Signal)	I_{B_OUTx}			± 20	mA
Gate Output Power Per Channel	P_{gx}			2	W
Switching Frequency	F_{SW}			20	kHz
Test Impulse Withstand Voltage Primary Side to Secondary Side (1.2 / 50 µs)[6-8]	$V_{IMP(PS)}$	acc. to IEC 60664-1:2020	4000		V_{PK}
Test Impulse Withstand Voltage Secondary Side to Secondary-Side (1.2 / 50 µs)[6-8]	$V_{IMP(SS)}$	acc. to IEC 60664-1:2020	2500		V_{PK}
Operating Voltage Primary Side to Secondary Side	V_{OP}	Transient only		1200	V_{PK}
Operating Voltage Primary Side to Secondary Side DC-Link Voltage	$V_{DC\text{-}Link}$	Permanently applied		1000	VDC
		Switching operation		950	VDC
Common Mode Transient Immunity	|dv/dt|		50		kV/µs
Storage Temperature[3]	T_{st}		-40	50	°C
Operating Ambient Temperature	T_A		-40	85	°C
Surface Temperature[4]	T_{SF}			85	°C
Operating Relative Humidity	H_R	No condensation		85	%
Altitude of Operation[5]	A_{OP}			5500	m

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. INx signals must statically be within the given limits. The transition from low-state to high-state and vice-versa must happen within 50 ns
3. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85 °C.
4. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value for coated gate driver versions to ensure long-term reliability of the coating material.
5. Operation above this level requires a voltage derating to ensure proper isolation coordination.
6. The on-board assembled gate driver IC SIC2192FQ is measured according to its datasheet.
7. All insulating subsystems are tested separately. The product insulation is not end of line tested.
8. The customer is requested to perform a high voltage test according to his product standard.

Recommended Operating Conditions

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Recommended Operation Conditions						
Primary Side Supply Voltage	V_{VCCx}	Referenced to GND	4.75	5	5.25	V
Gate Turn-On Voltage	$V_{GE,ON}$	Referenced to VEE		15		V
Gate Turn-Off Voltage	$V_{GE,OFF}$	Referenced to VEE		-5		V
Logic Low Input Voltage (Command Signals)	$V_{INx(L)}$	Referenced to GND			0.7	V
	$V_{ASC\_AD\_ENx(L)}$					
	$V_{ASC\_ADx(L)}$					
Logic High Input Voltage (Command Signals)	$V_{INx(H)}$	Referenced to GND	4.2			V
	$V_{ASC\_AD\_ENx(H)}$					
	$V_{ASC\_ADx(H)}$					
Logic Output Current SOx (fault signal)	I_{SOx}	V_{VCCx} = 5 V, R_{SOx} = 1.5 kΩ, open drain		- 3.3		mA
Switching Frequency	f_{SW}	2SP0215F2Q0C-FF900R12ME7W_B11			10	kHz

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Electrical Characteristics							
Logic Low Input Threshold Voltage (Command Signals)	$V_{INx(HL)}$	V_{VCCx} = 5 V, T_A = 25 °C, f_{SW} = 210 kHz			1.3		V
	$V_{ASC\_AD\_ENx(HL)}$ $V_{ASC\_ADx(HL)}$	V_{VCCx} = 5 V, T_A = 25 °C			1.3		V
Logic High Input Threshold Voltage Command Signals)	$V_{INx-(LH)}$	V_{VCCx} = 5 V, T_A = 25 °C, f_{SW} = 10 kHz			3.5		V
	$V_{ASC\_AD\_ENx(LH)}$ $V_{ASC\_ADx(LH)}$	V_{VCCx} = 5 V, T_A = 25 °C			3.5		V
Input Bias Current	I_{INx}	V_{VCCx} = 5 V, R_{INx+} = 1.53 kΩ			3.3		mA
	$I_{ASC\_AD\_ENx}$	V_{VCCx} = 5 V, $R_{ASC\_AD\_ENx}$ = 1.53 kΩ			3.3		
	I_{ASC_ADx}	V_{VCCx} = 5 V, R_{ASC_ADx} = 1.53 kΩ			3.3		
Supply Current (Primary Side)	I_{VCCx}	V_{VCCx} = 5 V, V_{INx} = 0 V		TBD	TBD	TBD	mA
		V_{VCCx} = 5 V, V_{INx} = 0/5 V, f_{SW} = 10 kHz		TBD	TBD	TBD	
Undervoltage Power Supply Monitoring Threshold (Primary Side)	$UVLO_{VCCx}$	Resume Operation		4.30	4.35	4.45	V
		Suspend Operation		3.85	4.12	4.20	
Undervoltage Power Supply Monitoring Blanking Time (Primary Side)	$UVLO_{VCCx(BL)}$	V_{VCCx} Voltage Drop from tbd to tbd		TBD	TBD	TBD	ns
Undervoltage Power Supply Monitoring Threshold (Secondary Side)	UVW_{VISOx}	Measured between V_{VISO} and V_{VEE}	Clear Warning	12.3	12.85	13.5	V
			Set Warning	11.6	12.3	13	
		Hysteresis		0.35	0.60	0.85	
Undervoltage Power Supply Monitoring Blanking Time (Secondary Side)	$UVW_{VISOx(BL)}$	V_{VISO} Voltage Drop from tbd to tbd		TBD	TBD	TBD	ns

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Electrical Characteristics (cont.)							
Overvoltage Power Supply Monitoring Threshold (Secondary Side)	OVW_{VISOx}	Measured between V_{VISO} and V_{VEE}	Clear Warning	17.3	18.5	19.8	V
			Set Warning	18	19.1	20.4	
		Hysteresis		0.3	0.6	0.84	
Power On Startup Time	t_{START}	The amount of time after primary and secondary side supply voltages reach minimal required level for gate driver proper operation.				TBD	ms
SENSE Fault Monitoring Blanking Time	$t_{SENSE(BL)}$			2.4		3.1	µs
Minimum Turn-On and -Off Pulses	$t_{GE(MIN)}$	All signals shorter then $t_{GE(min)}$ will be extended to $t_{GE(min)}$		33		1000	ns
Turn-On Propagation Delay	$t_{P(LH)}$	V_{INx} potential changes from 0 V to 5 V within 10 ns. Delay is measured from 50% voltage increase on <INx> pin to 10% voltage increase on GH pin T_J = 25°C Load: Module dependent[1]		TBD	TBD	TBD	ns
		V_{INx} potential changes from 0 V to 5 V within 10 ns. Delay is measured from 50% voltage increase on INx pin to 10% voltage increase on GH pin T_J = 85°C Load: Module dependent[1]		TBD	TBD	TBD	
Turn-Off Propagation Delay	$t_{P(HL)}$	V_{INx} potential changes from 5 V to 0 V within 10 ns. Delay is measured from 50% voltage decrease on INx pin to 10% voltage decrease on GL pin T_J = 25°C Load: Module dependent[1]		TBD	TBD	TBD	ns
		V_{INx} potential changes from 5 V to 0 V within 10 ns. Delay is measured from 50% voltage decrease on INx pin to 10% voltage decrease on GL pin T_J = 85°C Load: Module dependent[1]		TBD	TBD	TBD	
Gate Monitoring Turn-On Threshold	$V_{GM(ON)}$	$V_{GM(ON)} = V_{VISO} - V_{GL}$, V_{IN1} = 5 V, V_{IN2} = 0 V		2.8	3.1	3.4	V
Gate Monitoring Turn-Off Threshold	$V_{GM(OFF)}$	$V_{GM(OFF)} = V_{GH} - V_{COM}$, V_{IN1} = 0 V, V_{IN2} = 0 V		2.3	2.7	3.4	
Gate Monitoring Turn-On Delay	$t_{GM(ON)}$	The delay time between receiving a turn-on signal in the secondary side (corresponds to 50% rising time of GH signal) and (V_{VISO} - V_{VGL}) reaching $V_{GM(ON)}$		TBD	TBD	TBD	µs
Gate Monitoring Turn-Off Delay	$t_{GM(OFF)}$	The delay time between receiving a turn-off signal in the Secondary-side (corresponds to 50% falling time of GH signal) and (V_{VGH} - COM) reaching $V_{GM(OFF)}$		TBD	TBD	TBD	µs

Output Stage Overtemperature 1	$OT1_{GD}$	Setting Bit B_OUTx[18]	135	150	165	°C
Output Stage Overtemperature 2	$OT2_{GD}$	Setting Bit B_OUTx[17]	160	175	190	°C
Half-Bridge Dead-Time	t_{DT}		465	660	870	ns

NOTES:

1. Measured with typical modules. Time can be different (different module loads).

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Electrical Characteristics (cont.)						
DC/DC Controller Over Current Threshold	$I_{DCDC1(TH)}$	Setting Bit B_OUTx[25]	TBD	TBD	TBD	A
	$I_{DCDC2(TH)}$	Setting Bit B_OUTx[25]	TBD	TBD	TBD	
DC/DC Controller Over-Temperature	$OT1_{DCDC}$	Setting Bit B_OUTx[23]	135	150	165	°C
	$OT2_{DCDC}$	Setting Bit B_OUTx[24], Shutdown of DC/DC Controller Operation	160	175	190	
Internal TEMP Reference Voltage	V_{TEMP}	Internal reference current trimmed with an external resistor R_{TEMP}=400 Ohms connected between TEMP and COM pin	0.29	0.3	0.33	V
Internal TEMP Reference Current	I_{TEMP}		18.5	20	21	µA
TEMP Sampling Time	$t_{B\_OUT\_TEMP\_SAMPLING}$	The temperature output bit stream at B_OUTx is updated with a new temperature sampling within this period (8 x tB_OUT)	TBD	TBD	TBD	ms
SOx Output Voltage Logic Low	$V_{SO(0)}$	$V_{VCCx} \geq 3.9$ V, I_{SOx} = 3.4 mA, Referenced to GND	80	144	278	mV
SOx Fault Signalization Duration Time	t_{SO}	Duration of SO signal at low level during fault event	TBD	10	TBD	µs
SO Fault Signalization Delay Time	$t_{SO(dl)}$	Delay time to transfer faults from secondary-side to SO pin	TBD	165	TBD	ns

Parameter	Symbol	Conditions T_A = -40 °C to 85°C (Unless Otherwise Specified)		Min	Typ	Max	Unit
B_OUT Characteristics Channel 1 and 2							
Bit Length	t_{BIT}	Time from the beginning of one Bit to the beginning of the next Bit of the B_OUT signal		2.25	2.35	2.49	µs
Bit Pulse Width	t_{BIT0}	Percentage of B_OUT >Bit length t_{BIT}		72	73	74	%
	t_{BIT1}			45	47	50	
Bit Frame Transmission Rate	t_{B_OUT}	The transmission time from one data frame start Bit to the next data frame start Bit		588	615	631	µs
Data Word	B_OUT[idle]	Always Logic Low, Note 1		28			Bit
	B_OUT[1:29]	B_OUT[1]	Start Bit, Logic High		1		
		B_OUT[2:13]	Digitized TEMP Signal, B_OUT[2] = MSB, B_OUT[13] = LSB		12		
		B_OUT[14]	V_{VISO} Undervoltage Warning, Active Low		1		
		B_OUT[15]	V_{VISO} Overvoltage Warning, Active Low		1		
		B_OUT[16]	Gate Monitoring Warning, Active Low		1		
		B_OUT[17]	Over-Temperature Warning $OT2_{GD}$, Active Low		1		
		B_OUT[18]	Over-Temperature Warning $OT1_{GD}$, Active Low		1		
		B_OUT[19]	Secondary Side FluxLink™-out- of-Service Warning, Active Low Note 2		1		
		B_OUT[20]	Short Circuit Detection Fault, Active Low, Note 2		1		
		B_OUT[21]	Parity Bit of Secondary- to Primary Side Communication		1		
		B_OUT[22]	Primary Side FluxLink™-out-of-Service Warning, Active High		1		
		B_OUT[23]	Over Temperature Warning $OT1_{DCDC}$, Active High		1		
		B_OUT[24]	Over-Temperature Warning $OT2_{DCDC}$, Active High		1		
		B_OUT[25]	Primary Side DC/DC ControllerOver-Current Warning, Active High		1		
		B_OUT[26]	Not used, always Logic Low		1		
		B_OUT[27]	Dead-Time Insertion Warning,Active High		1		
		B_OUT[28]	Interlock Warning, Active High		1		
		B_OUT[29]	Stop Bit, Logic High		1		
B_OUT Output VoltageLogic Low	$V_{B\_OUT(0)}$	V_{VCC1} ≥ 3.9 V, I_{B_OUT} = 3.3 mA, Referenced to GND1		23	41	80	mV

1. The actual number of bit depends on the actual frame duration and may vary due to asynchronous transmission.
2. Always sent twice in 2 successive B_OUTx frame

Parameter	Symbol	Conditions T_A = -40 °C to +85 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Insulation Characteristics						
Creepage Distance between Primary- and Secondary Side	CPG_{P-S}	Outer layers, acc. to IEC 60664-1:2020, Table F.5, technical cleanliness considered	11			mm
	CPG_{S-S}	Outer layers, acc. to IEC 60664-1:2020, Table F.5, technical cleanliness not considered	6			
Clearance Distance between Primary- and Secondary Side	CLR_{P-S}	Outer layers, acc. to IEC 60664-1:2020, Table F.2, technical cleanliness considered, incl. altitude correction factor	4.9			mm
	CLR_{S-S}	Outer layers, acc. to IEC 60664-1:2020, Table F.2, technical cleanliness considered, incl. altitude correction factor	3			mm
Isolation Resistance, Input to Output	R_{IO}	V_{IO} = 500 V, 25 °C ≤ T_J ≤ $T_{A(MAX)}$	TBD			MΩ
	$R_{IO(S)}$	V_{IO} = 500 V at T_S[3] = 85 °C	TBD			
Isolation Capacitance, Input to Output	C_{IO}	V_{CIO} = 2 V, f_{CIO} = 1 MHz, T_A = 25 °C (Per channel)		10		pF
AC voltage test (dielectric withstand test)	V_{ISO}	According to IEC 60664-1:2020, 1s	3395			V_{RMS}
Input to Output Partial Discharge Extinction Voltage	$V_{PDext,PS}$	This test complies with partial discharge test (section 5.8.5) of IEC 60664-3:2016.	1591			V_{RMS}

Electrical Characteristics (EMI) Table						
Parameter	**Symbol**	**Conditions**	**Min**	**Type**	**Max**	**Unit**
Common-Mode Transient Immunity	$\|dV_{CM}/dt\|$	$\|V_{CM}\|$ = 1400VDC Static & Dynamic acc. VDE 0884-17 Note 1	±50			kV/µs
Variable MagneticField Immunity	H_{PEAK}	Aligned to ISO11452-8 / Test Level IV 15 Hz – 1 kHz: 1000 A/m 1 kHz – 10 kHz: 1000 A/m to 10 A/m 10 kHz – 150 kHz:10 A/m	TBD			
Radiated Immunity	E_{RAD}	Aligned to ISO11452-3 80 MHz – 1 GHz Note 2	TBD			V/m

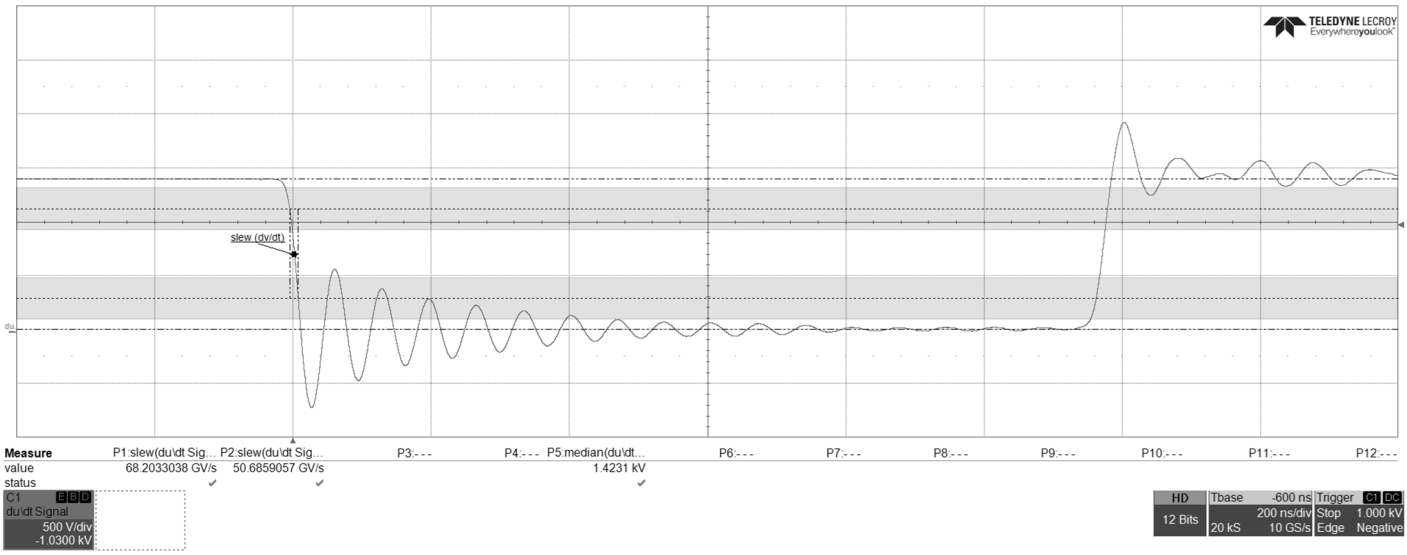


Figure 18 Applied Common Mode Pulses for Generating Positive dv/dt.

NOTES:
1. Tested signal path: IN+/IN-/ASD_AD/ASC_AD_EN to GH/GL and observed SO and B_OUT
2. Open PCB without shielding or housing

Technical Drawing

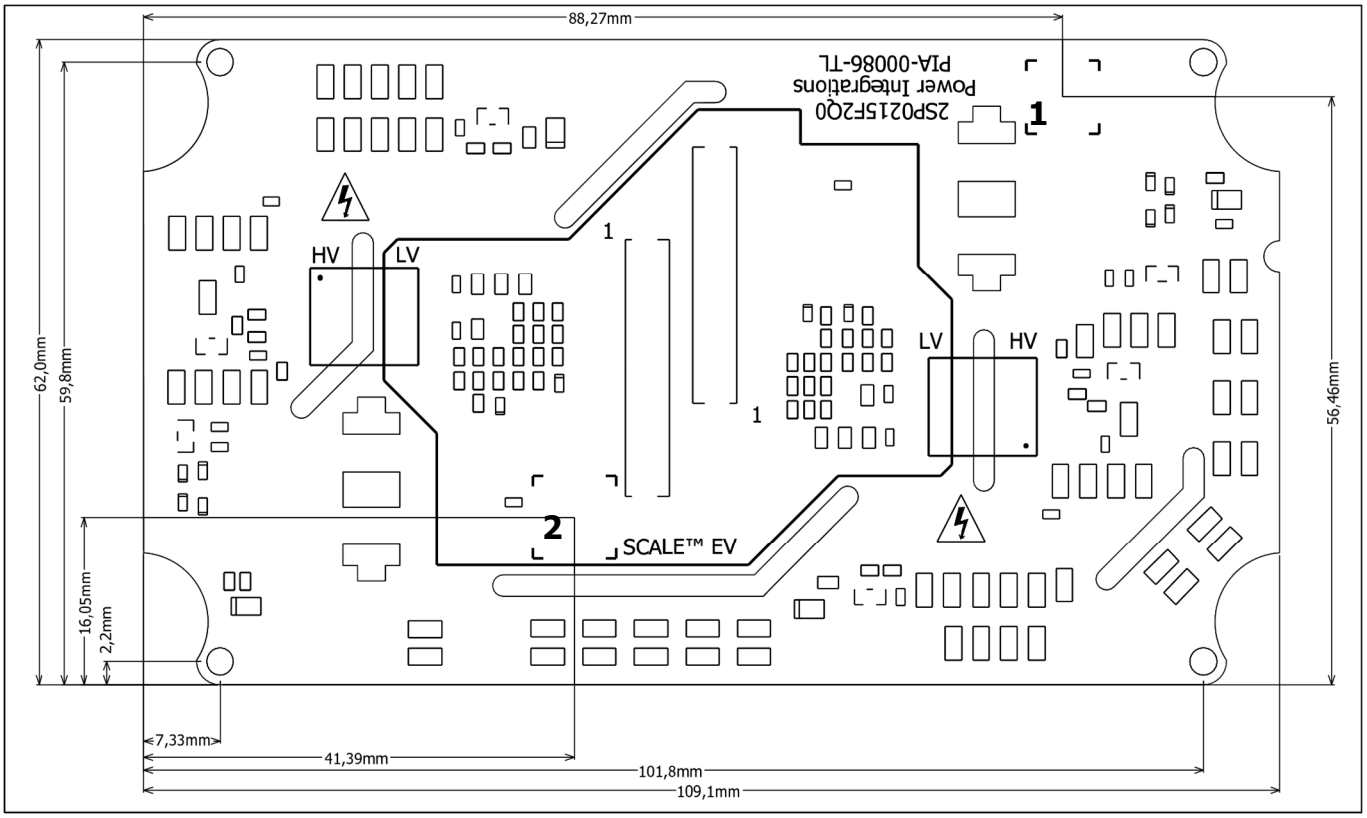


Figure 19. Technical Dimensions 2SP0215F2Q0C Gate Driver Board Top View

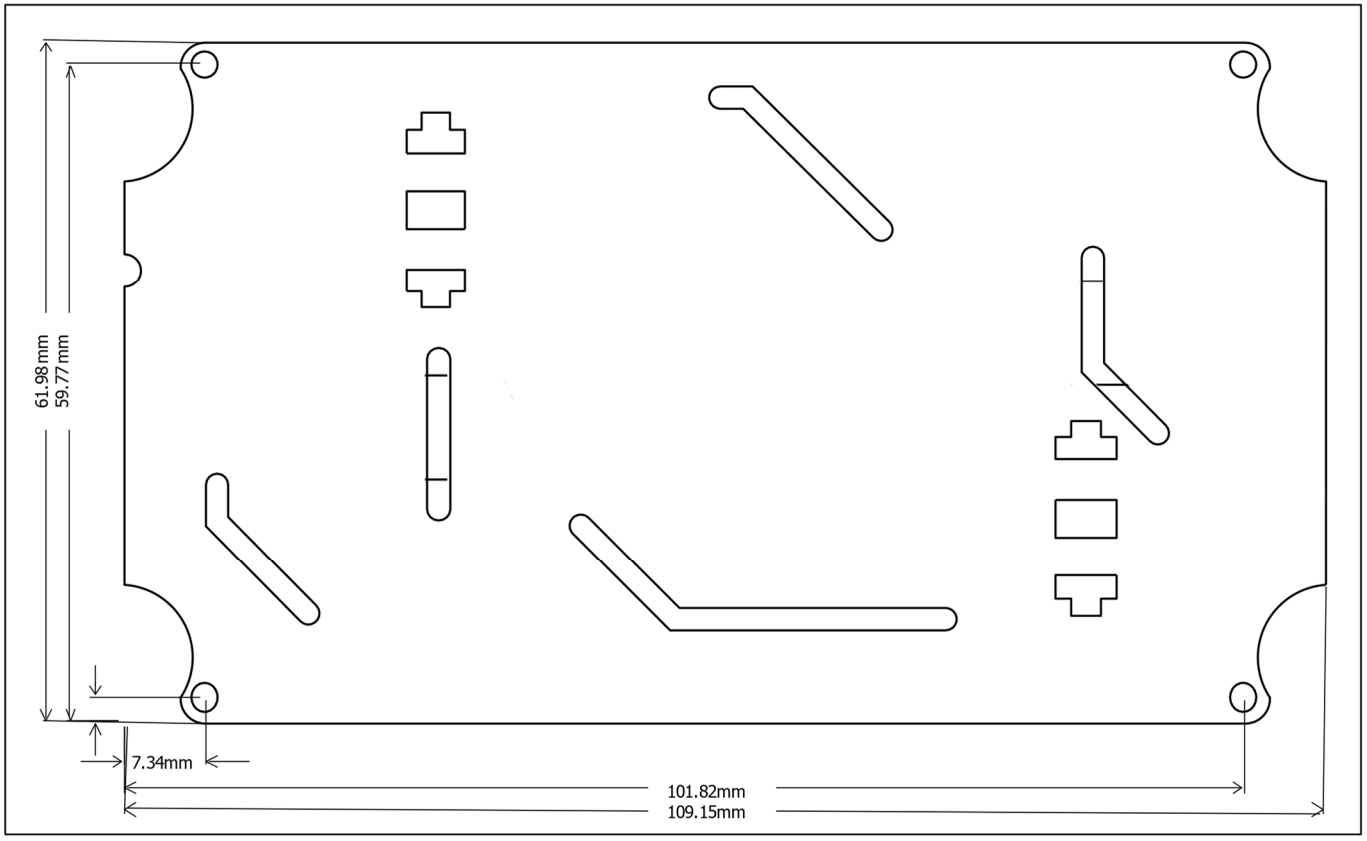


Figure 20. Technical Dimensions 2SP0215F2Q0C Gate Driver Board Bottom View

Mounting Instruction and PressFIT

PressFIT

The gate driver PCBA is mounted on top of the target IGBT module via a press fit connection to its gate, emitter, collector and NTC terminals.

PressFIT tool guidance and designs are available on request – please contact your local PI Sales office.

Cables

The cable from gate driver connector X300/X400 to the system level controller is not part of the 2SP0215F2Q0 gate driver and must be provided by the designer of the system. It is recommended to route the cable with minimum parasitic coupling from the controller to the gate driver. Parasitic coupling in particular to any potential of the secondary side of the gate driver (i.e. high voltage side) and the AC and/or DC bus bar must to be avoided. Otherwise, increased common-mode currents may circulate, which may cause interference with command, measurement and/or status feedback signals.

The following cables from Molex (see in Figure 21) are recommended for use and can be ordered under the product number 145132-0701.

Figure 21. Molex Micro-Fit 3.0 Connector Cable

Connector

The Molex Micro-Fit 3.0 vertical SMD 7 Pin connector on the board comes with 3.0 mm pitch, SMD solder tab on the sides for better mechanical stability, tin coated connector pins and glow-wire capable. This complies with the international standard IEC 60335-1 5th edition.

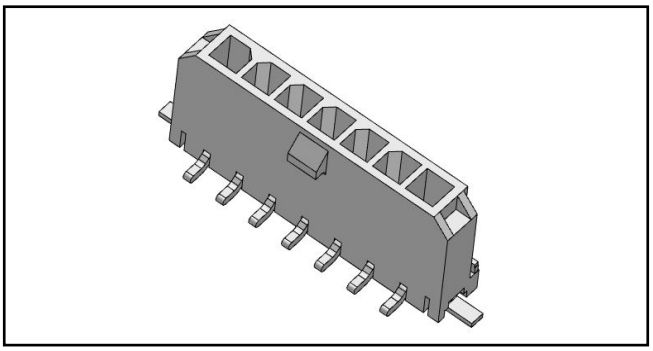


Figure 22. Molex Micro-Fit 3.0 Vertical 7 Pin Connector.

Isolation Distance between Gate Driver Boards

A minimum distance of 2 mm between gate driver boards and its IGBT module in the target application must be considered.

RoHS Statement

We hereby confirm that the product supplied does not contain any restricted substances according to Article 4 of the RoHS Directive 2011/65/EU more than the maximum concentration values permitted by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

Coating

The electronic components of the gate driver are protected by a layer of thick film UV-Curing coating. This coating increases product reliability when exposed to contaminated environments, especially conductive metal particles.

Note: Standing water (e.g. condensate water) on top of the coating layer must be avoided as this water will diffuse through the layer over time. Eventually it will form a thin film of conducting moisturee between PCB surface and coating layer, which will cause a rise in potentially harmful leakage currents. Such currents may lead to a disturbance of the performance of the gate driver.

Product Identification and Traceability Requirement

Data Matrix Codes (Traceability Label 1)

Product PCBA shall be labelled at location 1 as defined in Figure 19. The label is a standard for standard automated barcode readers. The information within the barcode is the serial number in the following format:

A204500002

- A = Supplier Traceability Designator (see PLM HP-Manufacturer)
- YY = Year, e.g. year 2020 is 20
- WW = work week (01 to 52)
- ZZZZZ = 5-digit unique serial number for the PCBA Reset every week (i.e. first sample from each week will have the 5 last digits as 00001).

Figure 23 – Details of Data Contained in Label at Location 1

Size of data matrix approx. 3x3 mm according to ECC 200 code size

The counting scheme shall follow base-36 which is hexadecimal, using 0 to 9 and A to Z.

The below table shows conversion examples and how base-36 is displayed in the 2D code. Note the unique serial number always contains 5 digits.

Decimals (base-10)	Base-36	Layout in 2D code marking
1	1	00001
13	D	0000D
500	DW	000DW
1'000	RS	000RS
9'999	7PR	007PR

Table 14 Conversion sample how the base-36 has to be displayed in the 2D code.

Part Number and Series Number Label 2

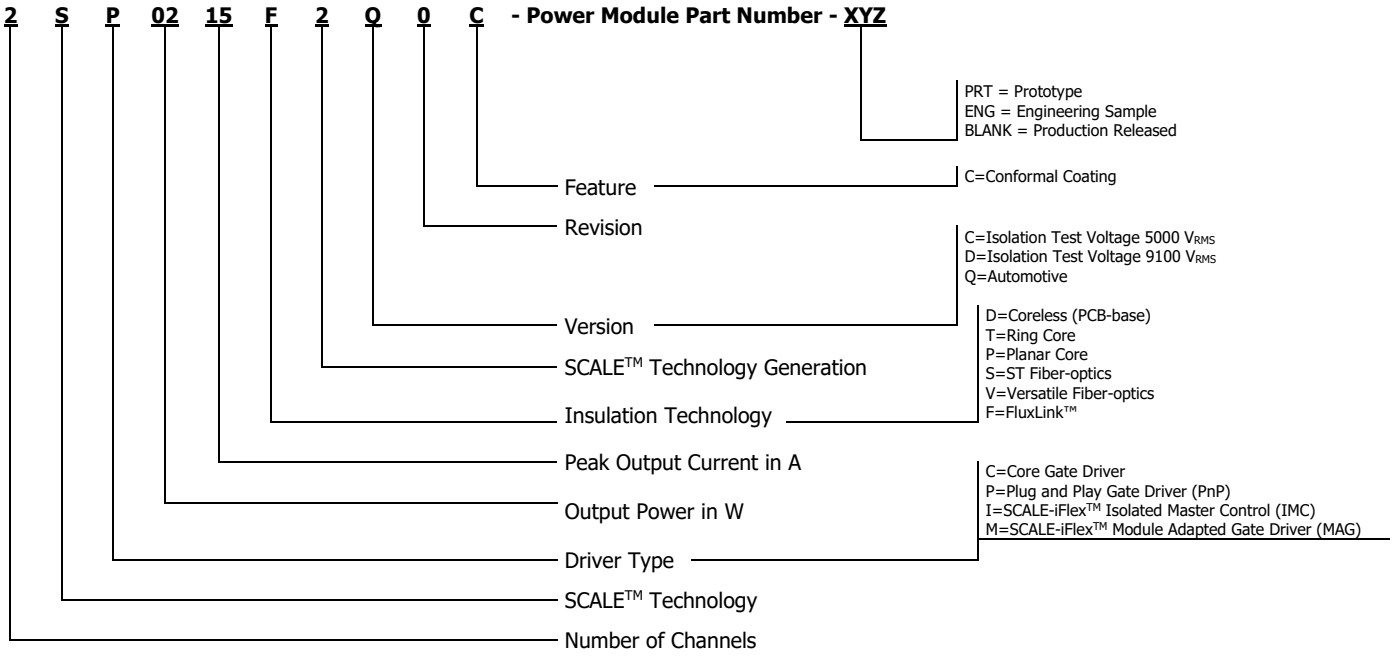
Product PCBA shall be labelled at location 2 as defined in Figure 1924. The label 2 is an ISO standard barcode reader label. The information within the barcode is the part number and serial number in the following format:

PPPYYWWZZZZZ

- PPP = 3 digits PLM Part Number = 2SP0215F2Q0C-FF900R12ME7W_B11
- YY = Year, e.g. year 2020 is 20
- WW = work week (01 to 52)
- ZZZZZ = 5-digit unique Ser. No. for the PCBA . Reset every week (i.e. first sample from each week will have the 5 last digits as 00001).

Figure 24 – Details of Data Contained in Label at Location 2

Part Ordering Information Table



Revision	Notes	Date
A	Target Specification	10/21
B	Target Specifciation Update	11/21
C	Preliminary release.	06/22
D	Preliminary release update	01/23

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Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA Main:
+1-408-414-9200
Customer Service: Worldwide:
+1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji
Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany
(AC-DC/LED/Motor Control
Sales) Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 3
59469 Ense Germany
Tel: +49-2938-64-39990
e-mail: igbt-
driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar Bangalore-
560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome
Bldg. 1-7-9, Shin-Yokohama,
Kohoku-ku Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail:
singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21 The
Westbrook Centre Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com