Design Example Report

Title	***40 W Multiple Output Flyback Converter With Four LED Drivers Using InnoMux™ IMX102U and InnoSwitch™ 3-MX INN3468C***
Specification	85 VAC – 265 VAC Input; 5 V / 3 A CV; (30 V – 50 V) / 25 W LED Output; 4 LED Strings
Application	Computer Display Monitor PSU
Author	Applications Engineering Department
Document Number	DER-636
Date	September 9, 2019
Revision	1.2

Summary and Features

Unique single stage conversion; multiple outputs; flyback architecture

- High full power efficiency across the universal line range
- Energy Star 8.0 efficiency compliance
- High accuracy independently regulated 5 V / 3 A CV output with extremely fast load transient response.
- Four independent CC LED outputs matched to within <3.5% at full current.
- Wide LED string voltage range: 30 V to 50 V makes it suitable for wide range of computer monitor applications.
- Configurable for
  - Analog dimming mode
  - Straight PWM dimming mode
  - Filtered PWM dimming mode
  - Hybrid dimming mode
- Control chipset incorporating isolated feedback and communication channels

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a PSU for a LED computer monitor. The 40 W PSU has a 5 V / 3 A CV output and a 25 W output providing power to four CC drivers intended for back-light LED strings in the LED monitor. The current through the individual LED strings is controlled from 0 mA to 156 mA by an analogue signal (ADIM) with a full scale of 1.5 V. The total maximum power output is 40 W and the input voltage range is 90 VAC to 265 VAC.

The PSU is based on a multiplexed, single-stage, multiple output topology shown in Figure 1. For each switching cycle, the energy stored in the transformer during the primary conduction interval is delivered to only one of the converter's main outputs (CV or LED). The energy from the primary is appropriately distributed between the converter main outputs by a secondary referred master controller according to the loading conditions at the outputs. This multiplexing is achieved by gating the steering FET Q1 appropriately. If energy pulse needs to be delivered to the CV1 output Q1 is turned ON prior to the end of the primary conduction interval. If Q1 is held OFF the energy is delivered to the LED output via the rectification diode D3. The master controller requests switching cycles from the primary as often as it needs to maintain all outputs in regulation. For the described multiplexing algorithm to work correctly it is essential that the transformer turns ratios are chosen such that: the minimum LED output voltage reflected to the primary of the transformer is greater than the CV output voltage reflected to the transformer primary. This technique achieves cross regulation within a fraction of 1% while significantly improving system efficiency when compared to conventional post regulation architectures. The new architecture supports multiple outputs driving both constant current and constant voltage loads, enabling the design of a single switch-mode power conversion stage that powers logic circuitry, USB ports, audio channels, and LED strings simultaneously.

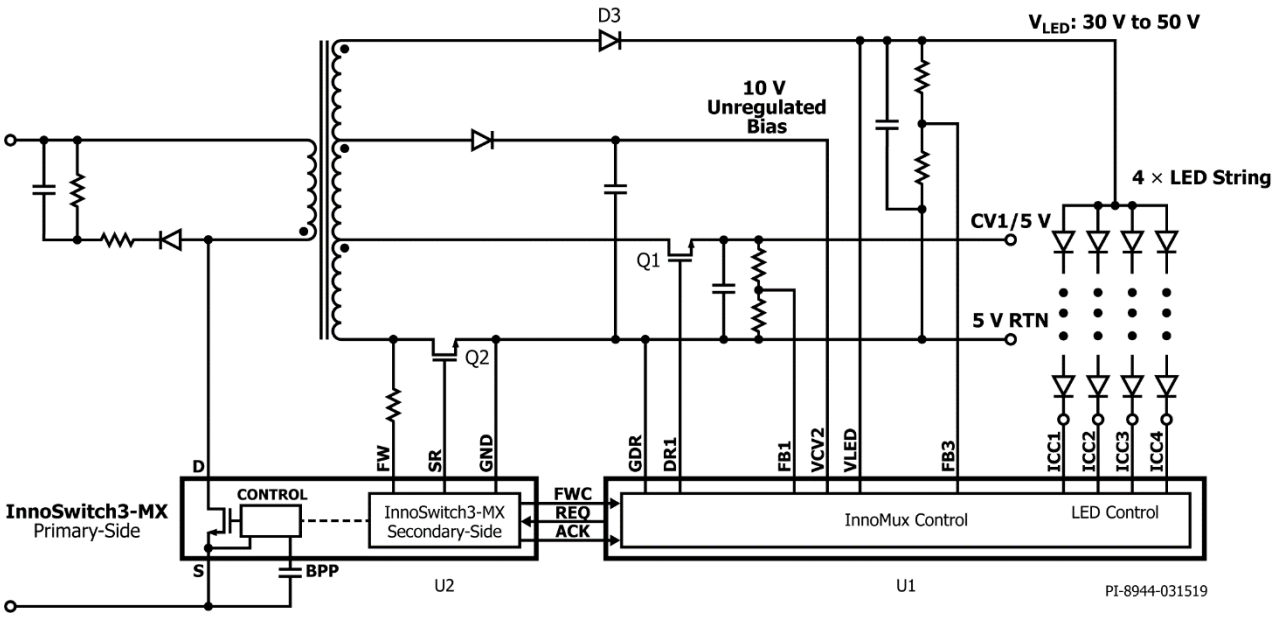

Figure 1 – Simplified Schematic of Multiplexed Architecture.

This novel architecture is implemented using two controller ICs, the InnoSwitch3-MX IC for primary switching plus SR FET control, and InnoMux IC for output voltage and current control. Selection MOSFET Q1 and D3 are used to direct the energy packet to either the CV or LED output respectively.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

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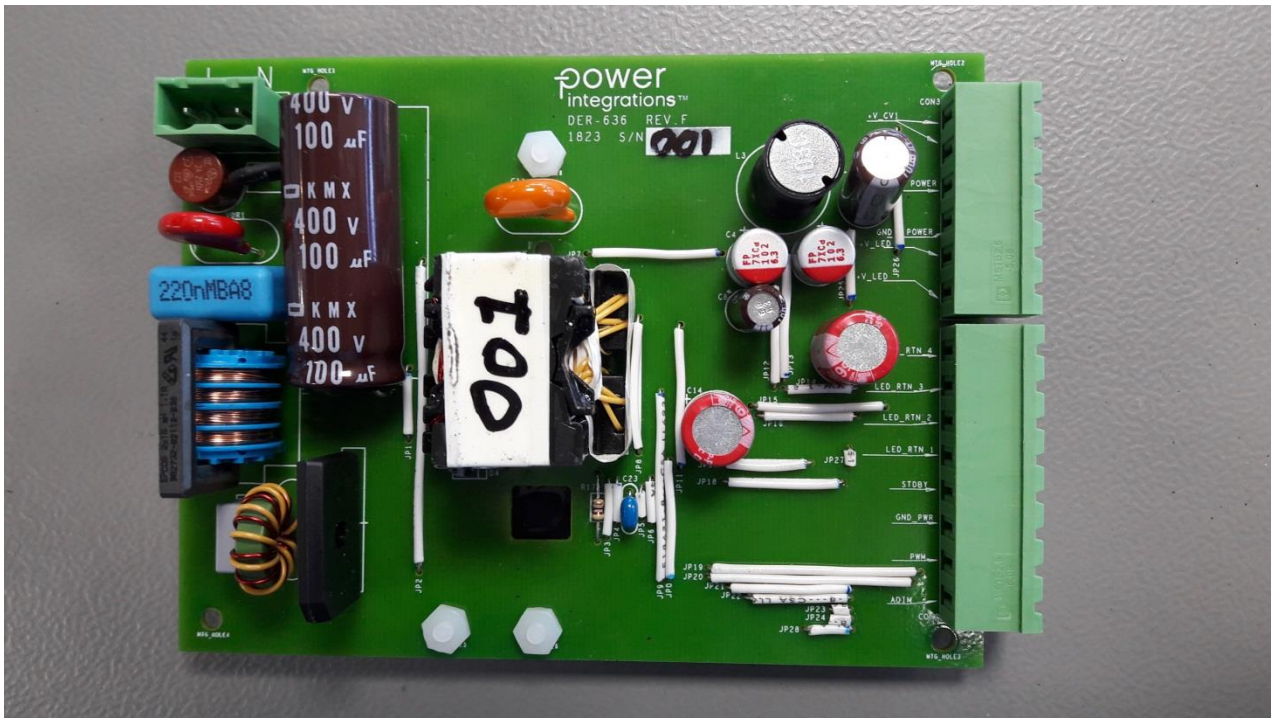

Figure 2 – PCB Assembly – Top View.

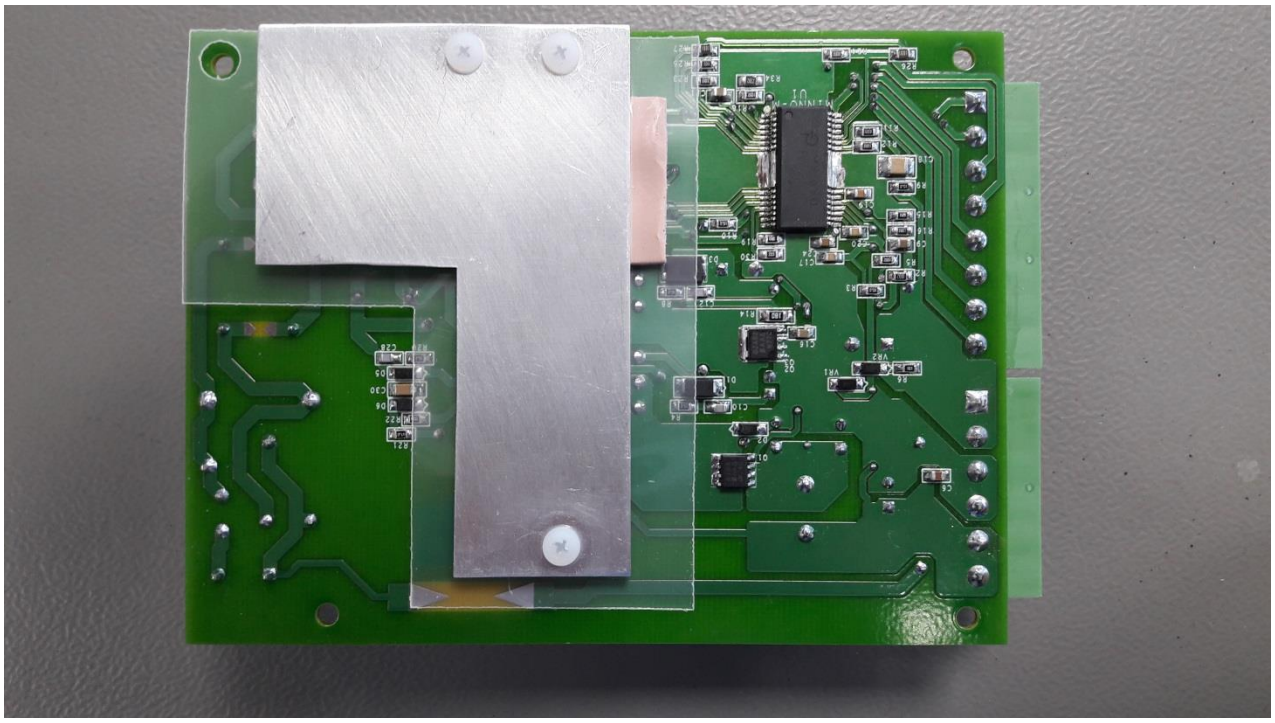

Figure 3 – PCB Assembly – Bottom View, with Heat Sink.

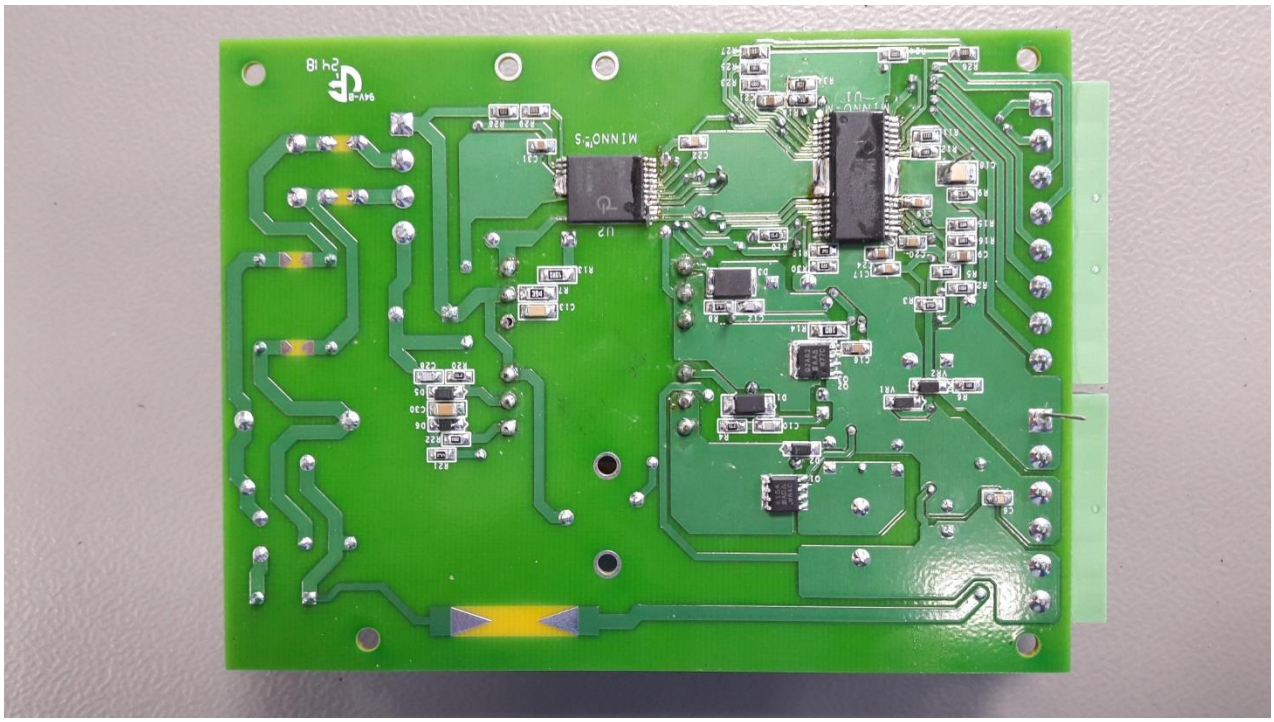

Figure 4 – PCB Assembly – Bottom View, without Heat Sink.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output Voltage CV1	V_{CV1}	4.75	5	5.25	V	±5%.
Output Ripple Voltage CV1	V_{RIPPLE_CV1}			50	mV	20 MHz Bandwidth.
Output Current CV1	I_{OUT_CV1}	0.0		3	A	
Output Voltage LED	V_{LED}	30	40	50	V	Max Power from LED Output is 25 W.
Output Current LED	I_{LED}	0		0.625	A	Total Current set for 40 V LED Panel with ADIM = 1.5 V
LED String Current Matching Error				3.5	%	Equal Voltage on all ICC Pins. 25 °C.
Total Output Power						
Continuous Output Power	P_{OUT}			40	W	
Efficiency						
Full Load	η	86			%	Measured at 110 VAC and 230 VAC, full load 5 V 3 A and 40 V 0.625 A.
Standby Input Power (LEDs off)				300	mW	Measured at 230 VAC 25 ºC, 5 V 15 mA, STDBY pin Pulled Low.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Common Mode Ring Wave		4		6	kV	100 kHz Ring Wave, 12 Ω. Common Mode.
Surge Combination Wave				1	kV	Combination Wave, 2 Ω Differential Mode.
ESD		±2		±15	kV	Air Discharge.
		±2		±8		Contact Discharge.
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

Table 1 - Power Supply Specification

3 Schematic

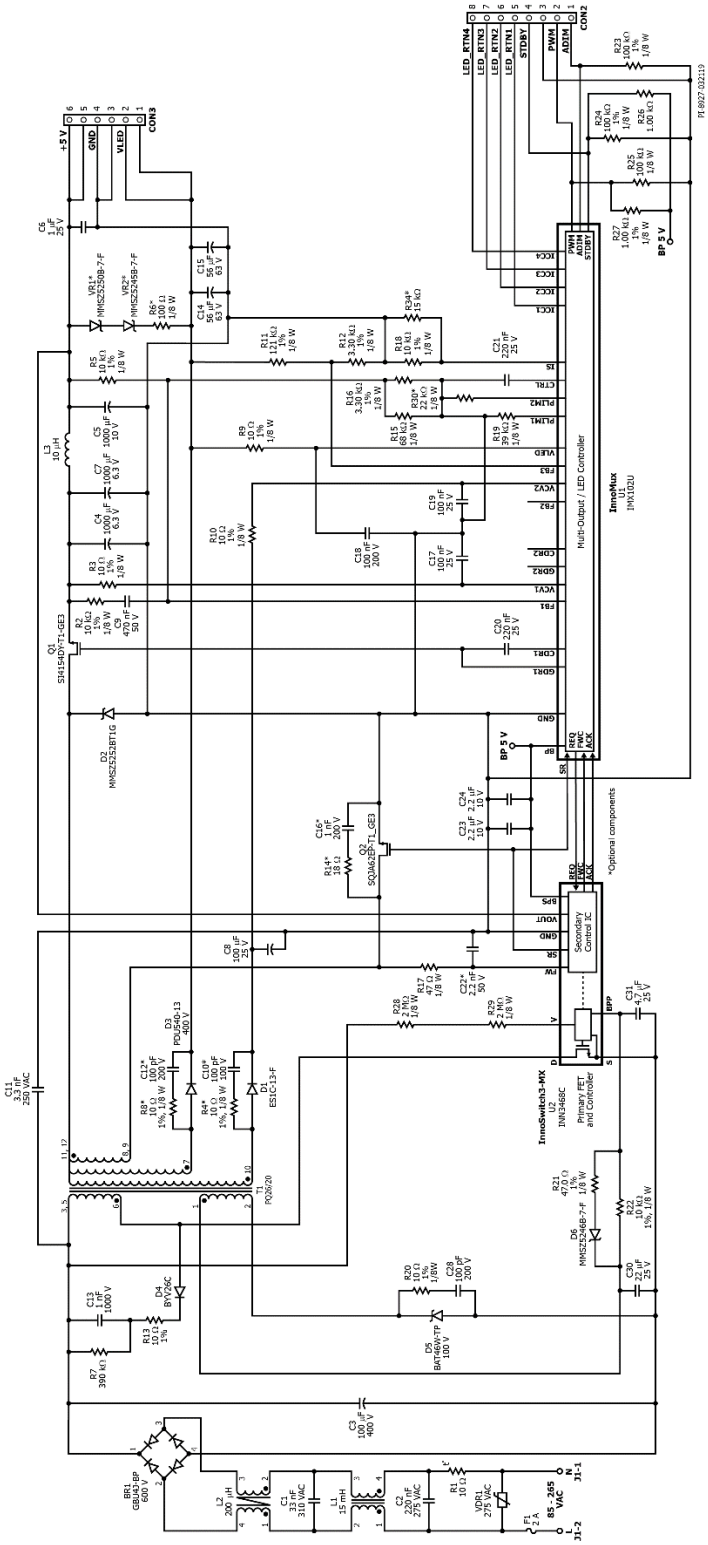

Figure 5 – Schematic.

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4 Circuit Description

4.1 Input EMI Filtering

A two-stage EMI filter is used on the line AC input, C2/L1 for lower frequencies and C1/L2 for high frequencies. Mainly common mode noise is suppressed by the input filter, but useful suppression of differential noise is also achieved. These measures along with the Y capacitor C11 and screens within the transformer constrain the conducted emissions to below the specification limits.

The bulk storage capacitor C3 provides DC voltage smoothing after the bridge rectifier. VDR R1 provides protection against differential voltage surges and the NTC R1 limits the inrush current at power up.

4.2 Primary-Side Conversion

See latest data sheet for InnoSwitch3-MX operation details

The transformer primary is connected between the rectified DC bus (VIN_DC_TX) and the drain of an integrated power MOSFET within InnoSwitch3-MX IC (U2 pin 24). Primary current is returned to the bulk capacitor (C3) via the source tab of U2 (pin 16).

A low cost RCD clamp, formed by D4, R13, R7 and C13, limits the peak drain voltage due to the effects of transformer leakage inductance and output trace inductance.

4.2.1 Primary-Side Controller Power Source and OVP Protection

The primary-side IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C31, when AC is first applied. During normal operation the primary-side of the controller is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D5 and capacitor C30, and fed into the BPP pin via a current limiting resistor R22.

4.2.2 Primary-Side OVP, Brown-In and Brown-Out Protection

The primary-side output overvoltage protection is obtained using Zener diode D6. In the event of an uncontrolled overvoltage at the output, the increased voltage at the bias winding cause the Zener diode D6 to conduct and trigger the OVP protection in the primary-side controller.

Resistor R28 and R29 provide line voltage sensing to provide controlled brown in/out behaviour, these are set to approximately 75 VAC and 65 VAC respectively. At approximately 320 VAC, the current through these resistors exceeds the line overvoltage threshold, which results in the disabling of U2.

4.2.3 Primary Peak Current Limit

Capacitor C31 is 4.7 μF which sets the primary-side controller peak current to 'Increased' i.e. 2.2 A.

4.3 Secondary-Side

See latest data sheet for InnoMux operation details

The secondary-side of the InnoSwitch3-MX IC (U2) is powered by the BP pin of the InnoMux IC (U1 pin 15) and decoupled by C2.

4.3.1 Primary to Secondary-Side Communication

The secondary-side of the InnoSwitch3-MX IC (U2) requests the primary-side to initiate a switching cycle via the FluxLink, a galvanically isolated control channel. This occurs when the InnoMux IC (U1) raises the REQ pin (U2 pin 1) to the appropriate level.

4.3.2 SR FET Control

The gate of the SR FET (Q2) is turned on based on the winding voltage sensed via R5 and the FW pin (U2 pin 9). In continuous conduction mode operation, the SR FET (Q2) is turned off just prior to the secondary-side controller requesting a new switching cycle from the primary side. In discontinuous mode the SR FET (Q2) is turned off when the voltage drop across the Q2 falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensures that the primary-side power MOSFET and SR FET are never turned on simultaneously. The SR FET gate drive signal is output on the SR pin (U2 pin7) and provides a 5 V drive, so a logic level MOSFET must be used.

4.3.3 InnoSwitch3-MX to InnoMux Communication

Communications between the InnoSwitch3-MX IC (U2) and the InnoMux IC (U1) is executed through the following:

REQ pin – this is an analogue multi-level request input from the InnoMux IC with the following values, assuming Vref=1.221 V from data sheet.

- <0.3 V – InnoMux IC is in reset.
- 0.3 V - 0.61 V – InnoMux IC is in idle ring measurement window mode.
- 0.61 V - 1.22 V – no pulse requested, but has control.
- 1.22 V - 2.44 V – pulse requested.
- >2.44 V – error, output overvoltage. Primary should be latched off.

ACK pin – On recognition of the switching cycle request from the InnoMux IC (U1), the InnoSwitch3-MX IC (U2) secondary-side, sends an acknowledge pulse to the InnoMux IC (U1). This is a digital signal.

The SR pin is used to drive the SR FET and allow the InnoMux IC (U1) to assess when the transformer is delivering energy to the secondary circuit.

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FWC pin – this is an indication of the total secondary discharge time. This is a digital signal from the InnoSwitch3-MX IC (U2) to the InnoMux IC (U1). Similar to SR signal, but indicates discharge time more completely as SR may be turned off early.

4.3.4 InnoMux Power Sources

See latest data sheet for InnoMux operation details

The InnoMux secondary-side control IC is powered by +V_LED during start-up via R9 and C18 (optional extra ESD supression) and VLED (U1 pin 23). An internal regulator reduces this to 5 V and outputs it on BP (U1 pin 15). Capacitor C24 provides BP5V decoupling for U1. The BP pin output powers the secondary-side controller of the InnoSwitch3-MX IC.

Once the voltage on VCV2 (U1 pin 21) reaches $VCV2_{MIN}$ (5.8 V - 8.0 V) the regulator input is switched from VLED to VCV2 to conserve power. VLED may be up to 100 V whereas VCV2 is usually 6 V – 12 V, the less voltage dropped, the lower the power loss. Resistor R10 and C19 provide optional extra ESD suppression. VCV2 is derived from an unregulated secondary winding in the transformer. The voltage generated by the winding depends on the loading conditions. Critically it provides a minimum of 5.8 V (at light load) supply to the CV2 pin.

4.3.5 High Side MOSFET Driver for Q1

The gate drive to the selection MOSFET Q1 provides a 5 V drive so a logic level MOSFET must be used. Capacitor C20 is charged up to the level of +V_CV1, 5 V in this case, then the –ve end of the capacitor is raised by 5 V, the BP level, to generate the 5 V gate drive pulse.
To allow visibility of the idle ring to the FW pin, Q1 is held on after a CV1 or VLED discharge cycle to permit Quasi Resonant switching when in DCM mode. During this time the InnoMux IC will send a REQ for the next pulse. When an ACK is received Q1 is turned off.

4.3.6 Output Control

Output rectification for the 5 V output is provided by SR FET (Q2) and CV1 selection MOSFET (Q1). Very low ESR capacitors, C4 and C7, provide filtering, and inductor L3 and capacitor C5 and C6 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the LED output is provided by SR FET (Q2) and diode (D3). Very low ESR capacitors, C14 and C15, provide energy storage and filtering at the LED output.

RC snubber networks comprising R14 and C16 for Q2, R8 and C12 for D3, R4 and C10 for D1 damp high frequency ringing across Diodes/MOSFETs, which results from leakage inductance of the transformer windings and the secondary's trace inductances.

Zener diode D2 is used as a voltage clamp for the transformer CV1 winding while the primary MOSFET is ON and Q1, Q2 are turned off, and D1, D3 are reverse biased. In this condition the secondary windings are floating w.r.t. GND. Without D2, the voltage on Q1 drain could be too high due to transformer winding capacitance interactions.

When the selection MOSFET (Q1) and the SR FET (Q2) are turned on, the transformer secondary windings are designed such that the voltage on the anode of D3 is below the lowest working LED string voltage. Therefore, D3 remains reverse biased and all the transformer energy is directed to the CV1 output via Q1.

When the selection MOSFET (Q1) is turned off and the SR FET (Q2) is turned on, the voltage on the anode of D3 rises until it is forward biased. In this condition all the transformer energy is directed to the LED output.

+V_CV1 output voltage is set by R5, R15 and R16 to FB1 (U1 pin 19). Loop compensation is provided by R2 and C9 due to the inclusion of L3.

+V_LED output overvoltage limit is set by R11 and R12 to FB3 (U1 pin 22). For DER-636 it has been set to 55 V.
Note: The actual +V_LED voltage is not set by these resistors, it is set by the voltage drop across the LED drivers ICC1-4, which is dependent on LED string current.

4.3.7 LED Current Control and Dimming

The LED current per driver is set by R18 and R34 on IS (U1 pin 3) plus, for this application which is configured for analog dimming, the voltage on ADIM (U1 pin 5). The resistance on the IS pin sets the maximum LED current per driver at the maximum ADIM voltage of 1.5 V. DER-636 has been set up for 625 mA total through 4 drivers with 1.5 V on ADIM, so 156.25 mA per driver.

Other dimming options are available, such as PWM, Sequenced PWM and combinations of analog and PWM. It would be simple to re-configure DER-636 to another dimming method. *See latest data sheet for InnoMux operation details.*

The InnoMux IC will auto detect the number of LED strings attached. To use a single string on DER-636, short outputs LED_RTN1 to 4, for 2 strings short LED_RTN 1 and 2 for the 1st string and short LED_RTN 3 and 4 for the 2nd string, for 3 strings leave LED_RTN 4 unconnected and connect the 3 strings to LED_RTN 1, 2 and 3. In the 3 string case, the IS resistors R18 and R34 will need adjusting to permit 625 mA total LED current if required. Each LED_RTN driver can conduct 240 mA maximum.

4.3.8 Output Power Limiting

A power limit is applied to each output individually by using the PLIM1 and PLIM2 pins (U1 pins 12 and 13). Power is restricted by limiting the maximum average frequency an

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output can receive charge pulses. That frequency is set by a resistor connected to the PLIM pin. In this case R19 on PLIM1 for the CV1 output and R30 on PLIM2 for the LED output. If the frequency is exceeded for a set period the InnoMux IC, and hence the whole circuit, will shut off and auto-restart.

4.3.9 Standby Mode

The STDBY pin is held at BP5V by R26. If STDBY is pulled to GND then the InnoMux IC enters 'Standby Mode'. Here, the LED driver circuit is powered down, reducing the InnoMux power requirement and the +V_LED output is maintained at a level of at least 15 V. With a standby load of 100 mW on +V_CV1, a Standby power at 230 VAC of under 300 mW can be realized.

Whilst in Standby Mode, full rated power (15 W) is still available on the +V_CV1 output.

Due to transformer leakage inductance there can be an overspill of energy into the LED winding that should go to the CV1 winding. With a low LED load (or no-load in Standby Mode) the LED voltage will increase, possibly to the OVP limit causing shut down. Zener diode VR1 and VR2 plus R6 dissipate some of the excess LED winding energy and passes the remainder to the CV1 output. Higher power LED operation and OVP function remain unaffected, but unwanted OVP operation is avoided in Standby.

Zener diode VR1 and VR2 may not be necessary if the transformer design has a low enough leakage inductance, or the application never allows a significant fraction of CV1 maximum power to be supplied during standby/very low LED current settings (say <20 mA).

4.3.10 Start-Up Process

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 8
Pri FET Vds [V]	CV1 5V Output [V]	V led Output [V]	BP5V [V]	U1/2 REQ pin [V]	U1/2 ACK pin [V]	LED Output Current [A]

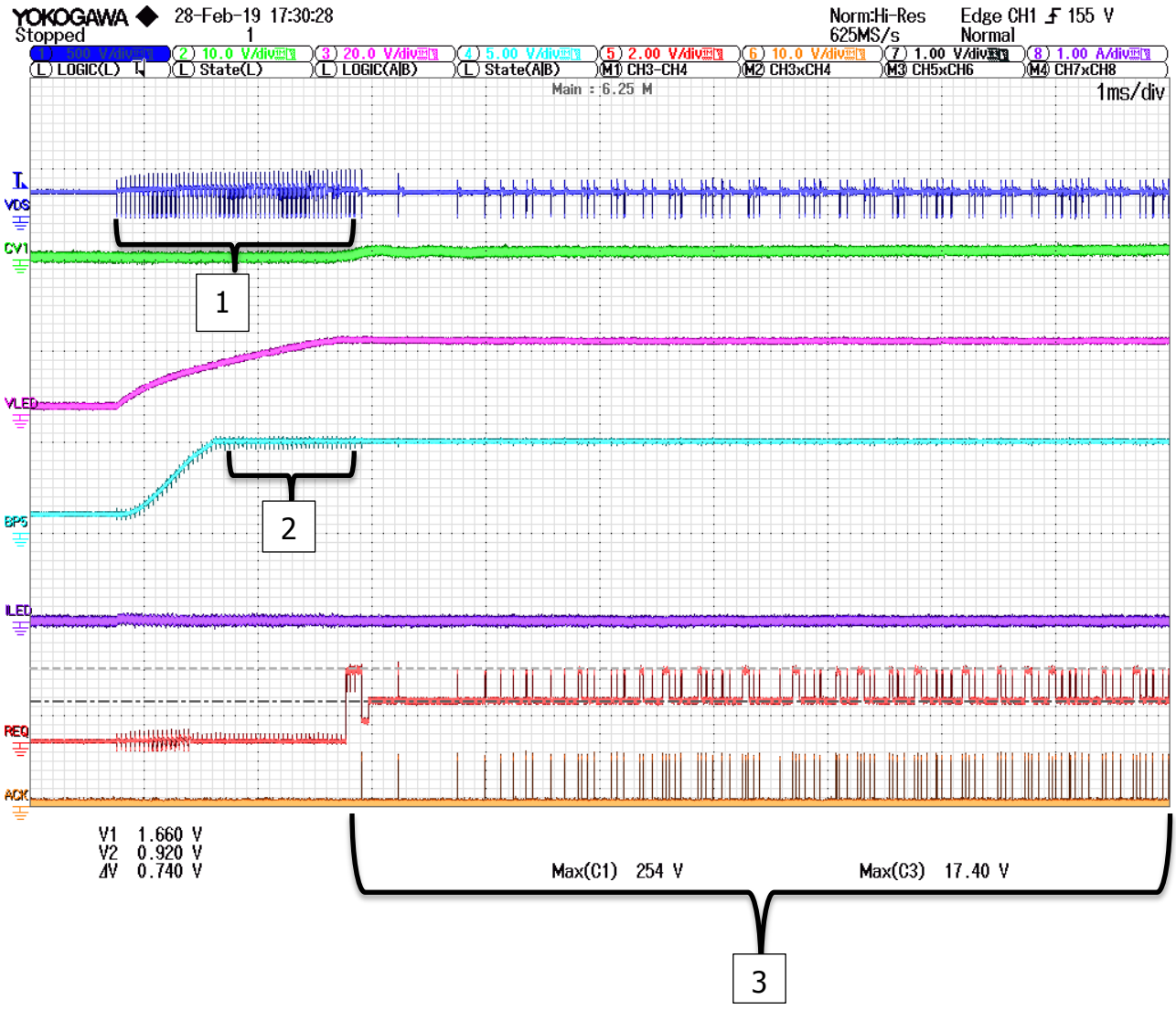

Figure 6 – First 10 ms of Start-Up.

1. Secondary-side controllers are un-powered or initializing, so the primary-side controller switches without feedback information at a default rate of about 25 kHz and peak current set to approximately 75% of the maximum level. If the secondary side is unresponsive the primary side will time out and shut down, or the primary side bias voltage will rise enough to trigger a bias OVP shutdown.

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2. The LED output is the only output to rise significantly during period [1]. Eventually it will rise to a level where the InnoMux IC (U1) internal series regulator can establish 5 V on BP5V. At this point U1 is drawing power only from the LED output via the VLED pin (pin 23). U2 is powered by U1 via the BP pin (U1 pin15). IC U1 and U2 secondary-side controllers then initialize and U1 raises the REQ pin (U1 pin 10) to request a pulse from the primary-side controller (~1.7 V).
3. When the InnoSwitch3-Mx secondary-side recognizes the signal, it requests a pulse from the primary-side and outputs an acknowledge pulse on the ACK pin (U2 pin 4). When the InnoMux IC (U2) recognizes the ACK signal, it drops the REQ pin to 'No Pulse Request' level (~0.9 V). The InnoMux IC (U2) then uses Q1 to direct a proportion of the flyback pulses to the CV1 output and the rest to the LED output.
4. CV1 and LED output voltages can be seen to rise somewhat together. At some time during period 4, the unregulated CV2 will reach a sufficient level to power U1 and U2 via the VCV2 pin (U1 pin 21). The U2 regulator will automatically switch to drawing power only via the VCV2 pin, which is a more efficient source.

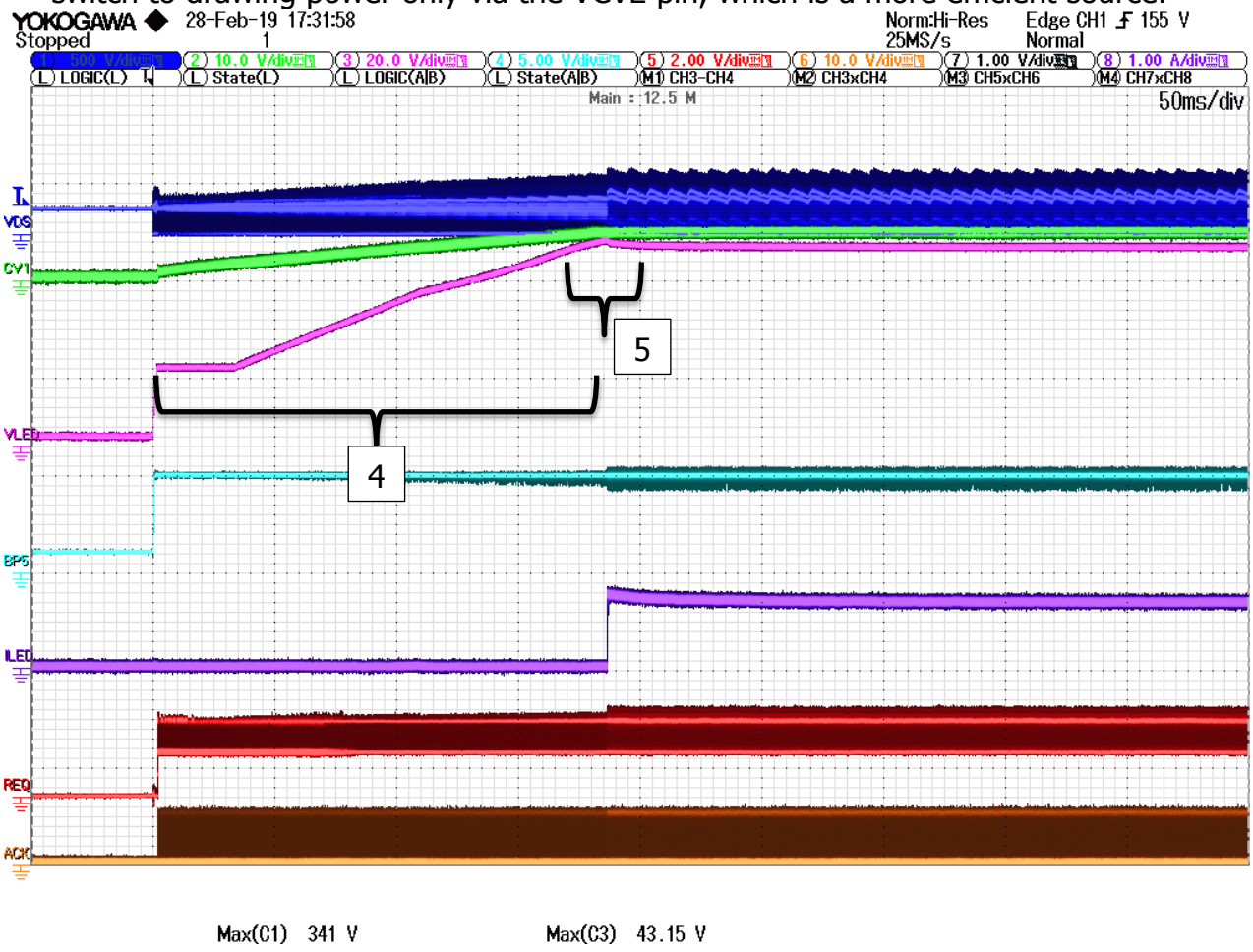

Figure 7 – Complete Start-Up Cycle Over Approximately 230 ms.

5. As the LED output voltage rises, a point will be reached when the forward volt drop of the LED strings will be exceeded, causing the voltage across the LED drivers (U2 pins 1, 2, 27 and 28) to rise. This is detected by the InnoMux controller and used to determine if there are any short circuit faults in the LED circuit. If a fault is detected then the circuit constantly shuts down and auto-restarts until the power or the fault is removed. If no faults are detected, the circuit will enter Stand-by mode (LEDs off) or normal mode (LEDs on), dependant on the level on the STDBY input (U2 pin 24).

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5 DER-636 Connection Diagram

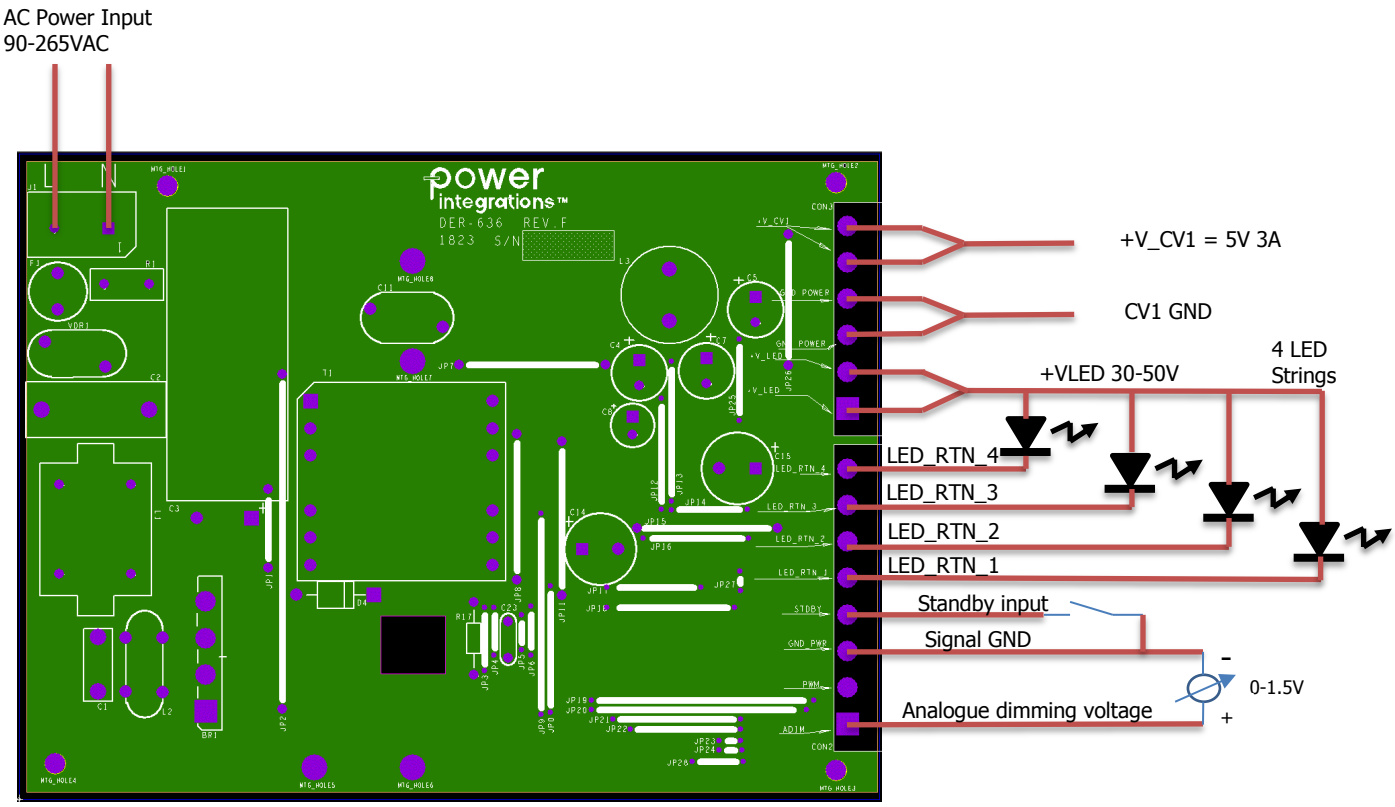

Figure 8 – DER-636 Connection Diagram.

6 PCB Layout

To minimize crosstalk between the outputs of the converter it is advisable to minimize the length of the connection between the negative terminals of C4 and C7 to the source of SR (Q2). The same applies to the connection from the negative terminals of C14 and C15 to the source of SR (Q2). The two AC paths to the SR source should be kept separate.

Ideally the connection between the GND pins of U1 and U2 should not be shared with any AC ripple current in the output filter stages. This is important for achieving accurate synchronous rectification.

The primary switch in InnoSwitch3-MX IC is cooled through the SOURCE pin (the paddle) of the IC. Care should be taken that the thermal impedance between the paddle and the cooling copper of the PCB is kept to a minimum. For best results the cooling copper pour should flair out as rapidly as possible away from the solder joint.

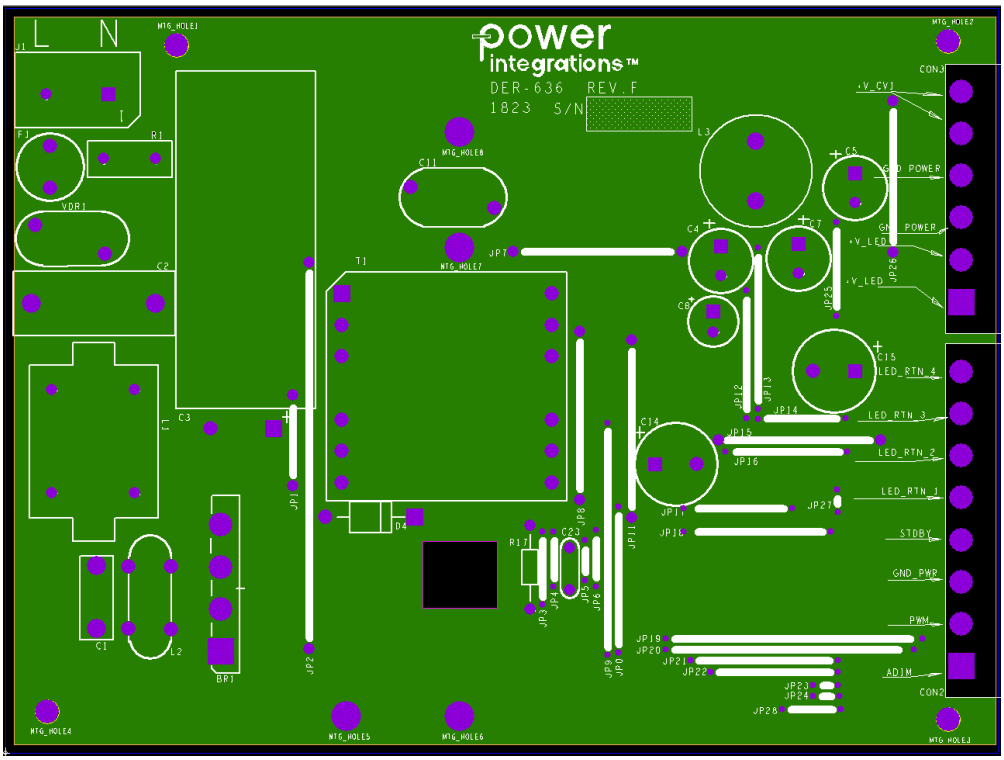

Figure 9 – Printed Circuit Layout, Top.

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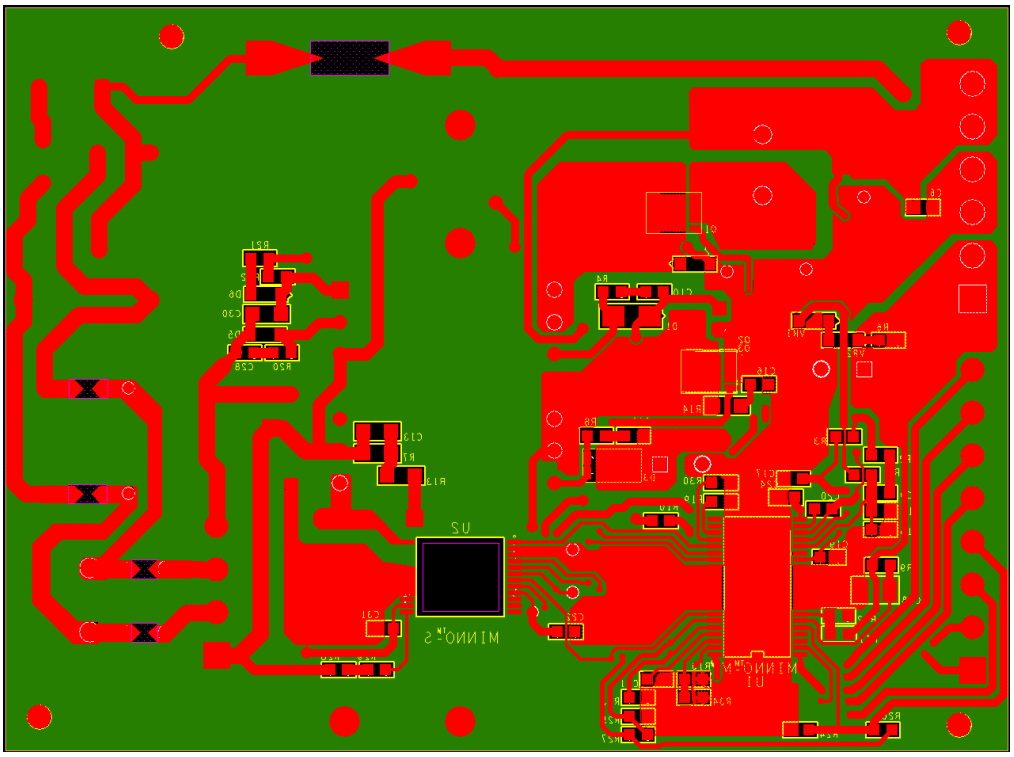

Figure 10 – Printed Circuit Layout, Bottom.

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 4 A, Bridge Rectifier, GBU Case	GBU4J-BP	Micro Commercial
2	1	C1	33 nF, 310 VAC, Polyester Film, X2	BFC233920333	Vishay
3	1	C2	220 nF, 275 VAC, Film, X2	PHE840MB6220MB12R17	Kemet
4	1	C3	100 µF, 400 V, Electrolytic, Low ESR, 630 mΩ, (16 x 40)	EKMX401ELL101ML40S	Nippon Chemi-Con
5	2	C4 C7	1000 µF,20%, 6.3 V, Al Organic Polymer, Gen. Purp, 2000 Hrs @ 105 °C, (8 x 8 mm)	RL80J102MDN1KX	Nichicon
6	1	C5	1000 µF, 10 V, Electrolytic, Very Low ESR, 41 mΩ, (8 x 20)	EKZE100ELL102MH20D	Nippon Chemi-Con
7	1	C6	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
8	1	C8	100 µF, 25 V, Electrolytic, Gen. Purp, (6.3 x 11)	EKMG250ELL101MF11D	Nippon Chemi-Con
9	1	C9	470 nF, 50 V, Ceramic, X7R, 0805	GRM21BR71H474KA88L	Murata
10	1	C10	100 pF 100V 10 % X7R 0805	08051C101JAT2A	AVX
11	1	C11	3.3 nF, Ceramic, Y1	440LD33-R	Vishay
12	2	C12 C28	100 pF, 200 V, Ceramic, COG, 0805	08052A101JAT2A	AVX
13	1	C13	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
14	2	C14 C15	56 µF, 20%, 63 V, Al Organic Polymer, Gen. Purp, (10 x 14)	870055875006	Wurth
15	1	C16	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
16	2	C17 C19	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
17	1	C18	100 nF, 200 V, Ceramic, X7R, 1210	12102C104MAT2A	AVX
18	2	C20 C21	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
19	1	C22	2.2 nF, 50 V, Ceramic, X7R, 0805	08055C222KAT2A	AVX
20	2	C23 C24	2.2 µF, 10 V, Ceramic, X7R, 0805	C0805C225M8RACTU	Kemet
21	1	C30	22 µF, 25 V, Ceramic, X5R, 1206	GRM31CR61E226KE15L	Murata
22	1	C31	4.7 µF, ±10%, 25 V, Ceramic, X7R, -55°C ~ 125°C, 0805	TMK212AB7475KG-T	Taiyo Yuden
23	1	CON2	CONN, TERM BLOCK, HDR, 5.08MM, 8 POS, 90º, Horizontal, RA	1757307	Phoenix Contact
24	1	CON3	CONN, TERM BLOCK, HEADER, 5.08 MM, 6 POS, 90º, Horizontal, RA	1757284	Phoenix Contact
25	1	D1	150 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1C-13-F	Diodes, Inc.
26	1	D2	Diode ZENER 24 V 500 mW SOD123	MMSZ5252BT1G	ON Semi
27	1	D3	Diode, Gen Purp, Fast Recovery =< 35ns, > 500 mA (Io), 400 V, 5 A,POWERDI5	PDU540-13	Diodes, Inc.
28	1	D4	600 V, 1 A, Ultrafast Recovery, 30 ns, SOD57	BYV26C	Philips
29	1	D5	Diode, SCHOTTKY, 100 V, 0.075 A, SOD123	BAT46W-TP	Micro Commercial
30	1	D6	Diode, ZENER 16 V 500 mW SOD123	MMSZ5246B-7-F	Diodes, Inc.
31	1	F1	2 A, 250 V, Slow, TR5	37212000411	Wickman
32	1	J1	2 Position (1 x 2) header, 7.5 mm pitch, Vertical	1766660	Phoenix
33	4	JP1 14 17 25	Wire Jumper, Insulated, #24 AWG, 0.5 in	C2003A-12-02	Gen Cable
34	1	JP2	Wire Jumper, Insulated, #24 AWG, 1.9 in	C2003A-12-02	Gen Cable
35	1	JP3	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
36	3	JP4 6 28	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
37	4	JP5 23 24 27	Wire Jumper, Insulated, #24 AWG, 0.2 in	C2003A-12-02	Gen Cable
38	5	JP7 8 13 15 26	Wire Jumper, Insulated, #24 AWG, 0.8 in	C2003A-12-02	Gen Cable
39	1	JP9	Wire Jumper, Insulated, #24 AWG, 1.1 in	C2003A-12-02	Gen Cable
40	4	JP10 12 18 21	Wire Jumper, Insulated, #24 AWG, 0.7 in	C2003A-12-02	Gen Cable
41	1	JP11	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable

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42	2	JP16 JP22	Wire Jumper, Insulated, #24 AWG, 0.6 in	C2003A-12-02	Gen Cable
43	2	JP19 JP20	Wire Jumper, Insulated, #24 AWG, 1.2 in	C2003A-12-02	Gen Cable
44	1	L1	15 mH, 1.1 A, Common Mode Choke	B82732R2112B30	Epcos
45	1	L2	200 µH, Common mode choke, 12 X 6 X 4		
46	1	L3	10 µH, Unshielded Wire Wound Inductor, 3.45 A, 15 mΩ Max, Radial, Vertical Cylinder	18R103C	Murata
47	8	MTG_HOLE1 - 8	Mounting Hole M 3		
48	1	Q1	MOSFET, N-Channel, 40 V, 36 A (Tc), 3.5 W (Ta), 7.8W (Tc), Surface Mount, 8-SO	SI4154DY-T1-GE3	Vishay
49	1	Q2	MOSFET, N-Channel, 60 V, 60 A (Tc), 68 W (Tc), PowerPAK® SO-8, PowerPAK SO-8	SQJA62EP-T1_GE3	Vishay
50	1	R1	NTC Thermistor, 10 Ω, 1.7 A	CL-120	Thermometrics
51	4	R2 R5 R18 R22	RES, 10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
52	6	R3 R4 R8 R9 R10 R20	RES, 10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
53	1	R6	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
54	1	R7	RES, 390 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ394V	Panasonic
55	1	R11	RES, 121 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1213V	Panasonic
56	2	R12 R16	RES, 3.30 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3301V	Panasonic
57	1	R13	RES, 10 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
58	1	R14	RES, 18 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ180V	Panasonic
59	1	R15	RES, 68 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ683V	Panasonic
60	1	R17	RES, 47 Ω, 5%, 1/8 W, Carbon Film	CF18JT47R0	Stackpole
61	1	R19	RES, 39 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ393V	Panasonic
62	1	R21	RES, 47.0 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF47R0V	Panasonic
63	1	R34	RED, 15 KΩ		
64	2	R23 R24	RES, 100 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
65	1	R25	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
66	2	R26 R27	RES, 1.00 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1001V	Panasonic
67	2	R28 R29	RES, 2 MΩ, 5%, 1/8 W, Thick Film, 0805	KTR10EZPJ205	Rohm
68	1	R30	RES, 22 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ223V	Panasonic
69	1	T1	Bobbin, PQ26/20, Vertical, 12 pins	B65877B0000R097 B65878E0012D001	TDK
70	1	U1	InnoMux - Multi output controller	IMX102U	Power Integrations
71	1	U2	InnoSwitch3-MX - Primary + Secondary side Flyback Controller	INN3468C	Power Integrations
72	1	VDR1	275 VAC, 45 J, 10 mm, RADIAL	V275LA10P	Littlefuse
73	1	VR1	DIODE ZENER 20 V 500 mW SOD123	MMSZ5250B-7-F	Diodes, Inc.
74	1	VR2	DIODE ZENER 15 V 500 mW SOD123	MMSZ5245B-7-F	Diodes, Inc.

Table 2 - DER-636 Bill of Materials

8 PI Expert Design Tool output

PI Expert is a continuously developing tool and later versions may give different, but improved results.

Inno_MUX_Flyback_122118; Rev.1.1; Copyright Power Integrations 2018	INPUT	INFO	Output	Unit	Description
Power Supply Basic Parameters					
VACMIN	90		90	[V]	Minimum Input AC Voltage
VACNOM			115	[V]	Nom. AC Voltage - universal designs low line
VACMAX			265	[V]	Maximum Input AC Voltage
PO			36.88	[]	Total Output Power
PO_MAX			40	[W]	Total Maximum Output Power
FL			50	[Hz]	Line Frequency
VMIN			86.9	[V]	Minimum Instantaneous DC Input Voltage at Min Mains
VMIN_AVG			105.8	[V]	Avarage input voltage calculated at VAC MIN
OUT_NUM			2		Select number of Outputs
DESIGN_RESULT			Design Passed		Design Result
Input Section					
CIN	**100**		100	[uF]	Input Capacitance
IAVG			0.51	[A]	Average Diode Bridge Current (DC Input Current)
CV Output Specification					
VO1			5	[V]	Output 1 Voltage
IO1			3	[A]	Output 1 Current
VO1_TOL_PCT			0	[%]	Output 1 Voltage tolerance
N1_PCT			86	[%]	Converter Efficiency for Output 1
Z1_PCT			60	[%]	Secondary loss allocation factor for Output 1
CONN1_TYPE	**AC_STACK**		AC_STACK		Winding connection type
LED Output Specification					
VO1			35	[V]	Output 2 Voltage
IO1			0.625	[A]	Output 2 Current
VO1_TOL_PCT			14.29	[%]	Output 2 Voltage tolerance
N1_PCT			86	[%]	Converter Efficiency for Output 2
Z1_PCT			60	[%]	Secondary loss allocation factor for Output 2
CONN1_TYPE	**AC_STACK**		AC_STACK		Winding connection type
Other Design Conditions					
VOR			87.27	[V]	Maximum Reflected Voltage Target
VOR_MARG_12			0.95		VOR Margin Between Output 1 and 2 reflected Voltage
KP_MIN	**1.018**		1.018		Min. Current Continuity Factor for Highest Voltage Output
Device Parameters					
DEVNAME	**INN3468**		INN3468		PI Device Name
DEVICE_MODE	**Increased**		Increased		Device Current Limit Mode
ILIMITTYP			2.2	[A]	Typical Current Limit
BVDSS	**650**		650		Main Switch Brake Down Voltage
Transformer Electrical Parameters					
LP_NOM			284.83	[uH]	Nominal Primary Inductance
LP_TOL	**2**		2	[%]	Primary Inductance Tolerance
NP	**24**		24		Calculated Primary Winding Total Number of Turns
BM_TESLA			0.22	[T]	Maximum Flux Density
BP_TESLA			0.23	[T]	Peak Flux Density
Transformer Mechanical Parameters					
CR_TYPE	**PQ26/20**		PQ26/20		Core Type

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BB_TYPE			PQ26/20 [NP],-1 (P6+ S6)		Bobbin Type
AE			119	[mm2]	Core cross section
BW			9.2	[mm]	Bobbin Winding Width
VE			5490	[mm3]	Core Volume
LG			0.278	[mm]	Estimated Gap Length
AL			6170		Ungapped Core Specific Inductance
ALG			494		Gapped Core Specific Inductance
Transformer Construction					
TRFCASE	**P1-S2-P2-S1**		P1-S2-P2-S1		
BSFF			84.6		Bobbin Stack Fill Factor
Primary Bias					
NB	**3**		3	Turns	Turns Primary Bias
STRBP			1	Strands	Primary Bias Winding - Strands
NBLP			1	Layers	Number of Primary Bias Layers
WIRETYPEBIASP	**Grade2_mm**		Grade2_mm		Primary Bias Wire Insulation Type
AWG_BIASP	**29**		29	[AWG]	Primary Bias AWG
WD_MM_BIASP			0.329	[mm]	Primary Bias Wire Diameter
CD_MM_BIASP			0.286	[mm]	Primary Bias Wire Copper Diameter
BFK_BIASP			11	[%]	Primary Bias Layer Fill Coeficient
NBS			1		Turns Secondary Bias
Primary winding					
NP	**24**		24	Turns	Total Number of Primary Turns
NP_SECT1			12	Turns	Primary first part - First Winding Section From The Core
NP_SECT2			12	Turns	Primary second part - Third Winding Section From The Core
WIRETYPE	**Grade2_mm**		Grade2_mm		Primary Winding Wire Insulation Type
STR	**2**		2	Strands	Primary Winding - Strands
NPL_P1			1	Layers	Primary first part Layers
NPL_P2			1	Layers	Primary second part Layers
AWG_P			28	[AWG]	Primary Winding AWG
WD_MM			0.367	[mm]	Primary Winding Wire Diameter
CD_MM			0.321	[mm]	Primary Winding Wire Diameter Copper Diameter
BFK			96	[%]	Primary Winding Layer Fill Coeficient
APSMM_ACT			5.35	[A/mm2]	Primary Actual Current Density
CV Output					
NS1_STACK			2	Turns	Output 1 Number of Turns
NS1	**2**		2	Turns	Sec. Winding 1 -Fourth Winding Section From The Core
WIRETYPE1	**TIW_mm**		TIW_mm		Sec. Winding 1 Wire Insulation Type
STR1	**3**		3	Strands	Sec. Winding 1 - Strands
NSL1			1	Layers	Sec. Winding 1 Layers
AWGS1	**22**		22	[AWG]	Secondary 1 Winding AWG
WDS1_MM			0.871	[mm]	Secondary 1 Winding Wire Diameter
CDS1_MM			0.644	[mm]	Secondary 1 Winding Wire Copper Diameter
BFK1			85	[%]	Secondary 1 Winding Layer Fill Coeficient
APSMM_ACT1			7.96	[A/mm2]	First Secondary Winding Actual Current Density
LED Output					
NS2_STACK			9	Turns	Output 2 Number of Turns
NS2	**11**		11	Turns	Sec. Winding 2 - Fifth Winding Section From The Core
WIRETYPE2	**TIW_mm**		TIW_mm		Sec. Winding 2 Wire Insulation Type
STR2			1	Strands	Sec. Winding 2 - Strands
NSL2			1	Layers	Sec. Winding 2 Layers
AWGS2	**24**		24	[AWG]	Secondary 2 Winding AWG
WDS2_MM			0.739	[mm]	Secondary 2 Winding Wire Diameter

CDS2_MM			0.511	[mm]	Secondary 2 Winding Wire Copper Diameter
BFK2			80	[%]	Secondary 2 Winding Layer Fill Coeficient
APSMM_ACT2			7.18	[A/mm2]	Second Secondary Winding Actual Current Density
Operating Parameters Worst case					
FS			77529	[Hz]	Maximum Operating Switching Frequency
FS_MIN			56815	[Hz]	Minimum Operating Switching Frequency
KRPKDP			0.79		Minimum Current Continuity Factor
VOR_ACTUAL			87.27	[V]	Actual Maximum Reflected Voltage
VOR_MARG_12_ACT			0.92		VOR Margin Between Output 1 and 2 reflected Voltage
VOR_MARG_12MAX_ACT			0.69		VOR Margin Between Output 1 and Output 2 maximum reflected Voltage
DMAX			0.5		Maximum Duty Cycle (at VMIN and full load)
TON			7.28	[us]	Maximum Controller ON Time (at VMIN and full load)
TOFF			6.73	[us]	Minimum Controller OFF Time (at VMIN and full load)
VDRAIN			462	[V]	Off state drain to source voltage
VDS			0.5	[V]	On state Drain to Source Voltage
IP			2.18	[A]	Peak Primary Current (at VMIN and full load)
IRMS			0.87	[A]	Primary RMS Current (at VMIN and full load)
ISRMS1_STACK			7.78	[A]	Secondary 1 Winding RMS Current
ISRMS1_STACK			1.47	[A]	Secondary 2 Winding RMS Current
PTRFLOSS_TOT			0.94	[W]	Total Transformer Power Loss
PTRFLOSS_WIND			0.36	[W]	Transformer Windings Power Loss
PTRFLOSS_CORE			0.57	[W]	Transformer Core Power Loss
Output Parameters (Worst case)					
CV Output					
VO1			5	[V]	Output 1 Voltage
IO1			3	[A]	Output 1 Current
PO1			15	[W]	Output 1 Power
PO1_MAX			15	[W]	Output 1 Maximum Power
VD1			0	[V]	Estimated Forward Voltage across Output Diode
KP1			0.79		Current Continuity Factor during Output 1 Conduction
DMAX1			0.41		Duty Cycle during Ouput 1 Conduction
ISP1			26.15	[A]	Secondary Peak Current during Ouput 1 Conduction
ISRMS1			7.64	[A]	Output 1 RMS Current
IRIPPLE1			7.03	[A]	Output 1 Capacitor - RMS Ripple Current
CV Output Components					
VO1_RIPPLE			0.1	[V]	Output 1 Ripple Voltage
COUT1			1031.87	[uF]	Minimum Output Capacitance Required
RESR			0.05	[Ohm]	Output 1 Capacitor ESR Value
PLOSS_COUT1			2.47	[W]	Output 1 Capacitor ESR losses
VZ0_CLAMP			10.91		Minimum Zener 1 Clamp Voltage
OSR1_PIVS			42.14	[V]	Synch.Rectifier 1 Voltage
OSR1_RDSON			0.01	[Ohm]	Sync.Rectifier 1 ON Resistance
PLOSS_SR1			0.58	[W]	Sync.Rectifier 1 Conduction Losses
OSF1_PIVS			10.91	[V]	Selection FET 1 Minimum Voltage
OSF1_RDSON			0.01	[Ohm]	Selection FET 1 ON Resistance
PLOSS_SF1			0.58	[W]	Selection FET 1 Conduction Losses

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LED Output					
VO1			35	[V]	Output 2 Voltage
IO1			0.63	[A]	Output 2 Current
PO1			21.88	[W]	Output 2 Power
PO1_MAX			25	[W]	Output 2 Maximum Power
VD1			0	[V]	Estimated Forward Voltage across Output 2 Diode/Rectifier
KP1			1.02		Current Continuity Factor during Output 2 Conduction
DMAX1			0.5		Duty Cycle during Ouput 2 Conduction
ISP1			4.74	[A]	Secondary Peak Current during Ouput 2 Conduction
ISRMS1			1.47	[A]	Output 2 RMS Current
IRIPPLE1			1.33	[A]	Output 2 Capacitor - RMS Ripple Current
LED Output Components					
VO1_RIPPLE			0.1	[V]	Output 2 Ripple Voltage
COUT1			133.45	[uF]	Minimum Output 2 Capacitance Required
RESR			0.05	[Ohm]	Output 2 Capacitor ESR Value
PLOSS_COUT1			0.09	[W]	Output 2 Capacitor ESR losses
PIVS1			180.54	[V]	Output 2 Diode Voltage
OSF1_RDSON			-	[Ohm]	Selection FET 2 ON Resistance
PLOSS_SF1			-	[W]	Selection FET 2 ON Losses
PLOSS_OD1			0	[W]	Output Diode 2 Losses
Primary Bias					
NB	**3**		3		Primary Bias Winding Turns
VB	**14**		14	[V]	Primary Bias Voltage at maximum load
VF_BIAS			0.7	[V]	Primary Bias Voltage Forward Drop
VREVERSE_BIASP			60.85	[V]	Primary Bias Reverse Voltage
CBIAS			22	[uF]	Primary Bias Capacitor
VSB			-		Secondary Bias Voltage
NBS			1		Turns Secondary Bias
VF_BIASS			0.7	[V]	Secondary Bias Rectifier Voltage Forward Drop
VREVERSE_BIASS			54.35		Secondary Bias Rectifier Reverse Voltage
Tolerance Analysis					
Output_Index	**One**		One		Output to be displayed
VO1_VO2_VO3_Corner	**nom-nom-nom**		nom-nom-nom		VO tolerance corner to be dispalyed
ILIMIT_LP_Corner	**nom-nom**		nom-nom		Curr.Limit/Inductance combination to be dispalyed
VOUT1_ACTUAL			5	[V]	Actual Output Voltage
VOR1			60	[V]	Reflected voltage
IO1			3	[A]	Output Current
PO1_ACTUAL			15	[W]	Actual Output Power
FS1			65502.43	[Hz]	Switching frequency
DMAX1			0.4		Duty cycle
KP1			0.92		Current Continuity Factor
TON1			6.15	[us]	Controller ON Time
TOFF1			9.12	[us]	Controller OFF Time
IP1			2.09	[A]	Primary peak current
ISRMS1			7.44	[A]	Secondary RMS Current
IRIPPLE1			6.81	[A]	Output Capacitor - RMS Ripple Current
BM			2084.24	[Gauss]	Maximum Flux Density (Steady State Condition)
BP			2194.06	[Gauss]	Peak Flux Density (@ 132kHz - transitory condition)
IRMS_AVG			0.769	[A]	Primary RMS current at VMIN AVG (VO1=Nom, VO2=Nom, VO3=Max) or (VO1=Nom, VO2=Max)

Errors, Warnings, Information					
IDS_INFO			-		Although the design has passed the user should validate functionality on the bench. Please check the variables listed.
IDS_WARN			-		Design variables whose values exceed electrical/datasheet specifications.
IDS_ERR			-		The list of design variables which result in an infeasible design.

Table 3 - PI Expert Design Tool output

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9 Transformer (T1) Specification

9.1 Electrical Diagram

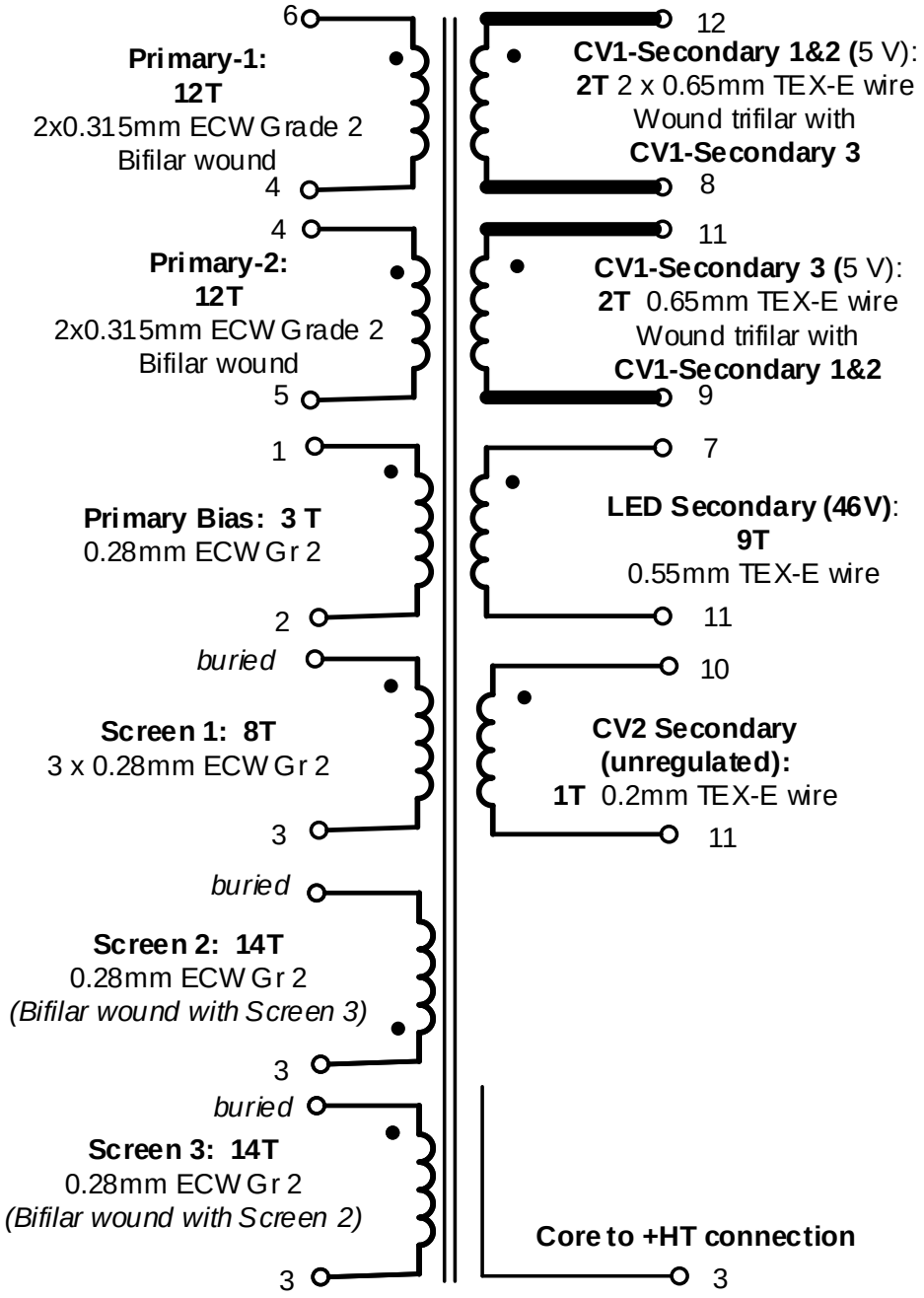

Figure 11 – Transformer Electrical Diagram.

9.2 Winding Stack Diagram

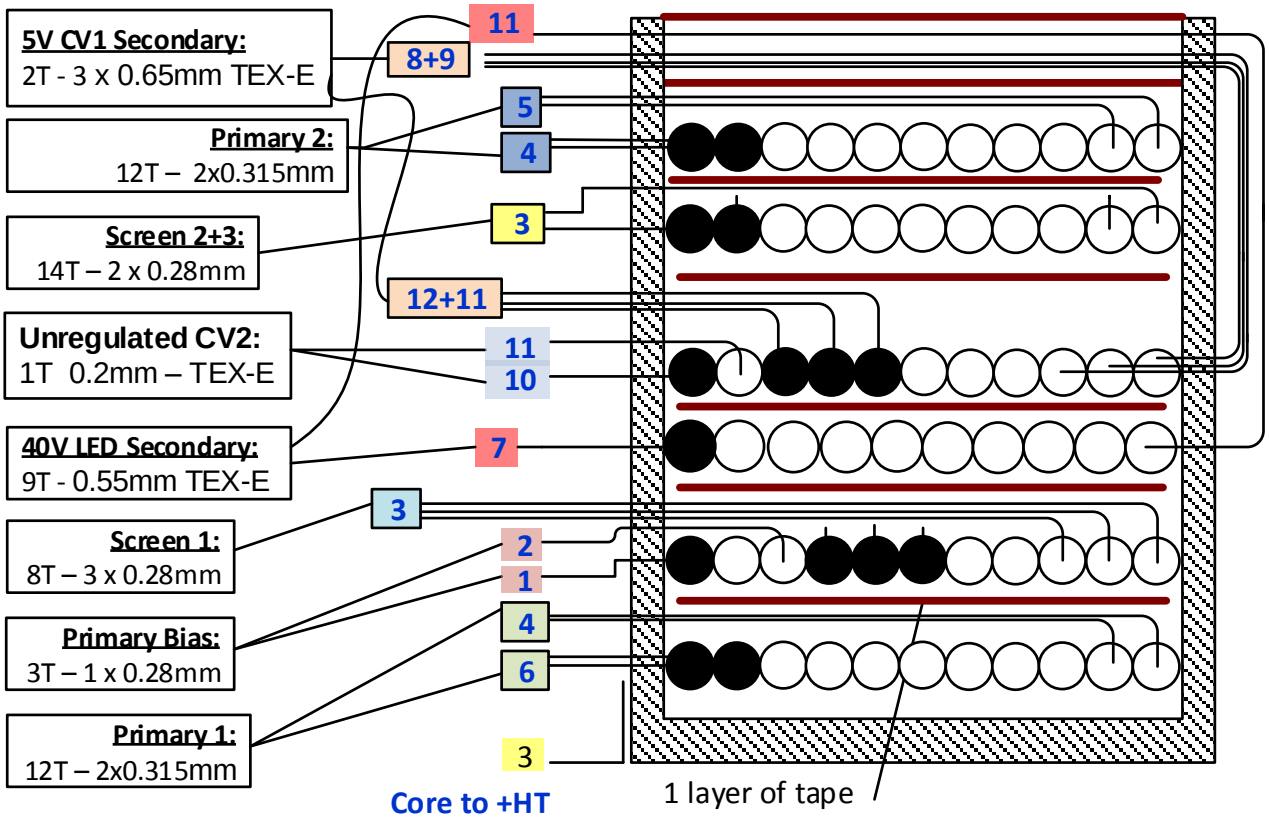

Figure 12 – Transformer Winding Stack

9.3 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 3, 4, 5, 6 and FL0 to pins 7, 8, 11 and 12.	3000 VAC
Primary Inductance	Pin 5 – pin 6, all other windings open, measured at 10 kHz, 0.4 V_{RMS}.	285 µH ±3%
Resonant Frequency	Pin 5 – pin 6, all other windings open	1100 kHz (Min.)
Primary Leakage Inductance	Pin 5 – pin 6, with pins 7, 8 and 9 shorted and, 11 and 12 shorted, measured at 10 kHz, 0.5 V_{RMS}.	4 µH (Max.)

Table 4 - Transformer Electrical Specifications

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9.4 Materials List

Item	Description
[1]	Core: PQ26/20, N97, TDK – B65877B0000R097.
[2]	Bobbin: TDK – B65877BE0012D001. PQ26/20 bobbin with extended skirt between pin rows.
[3]	TEX-E Wire: 0.65 mm Triple Insulated.
[4]	TEX-E Wire: 0.55 mm Triple Insulated.
[5]	TEX-E Wire: 0.2 mm Triple Insulated.
[6]	Magnet Wire: 0.315 mm, Grade 2 ECW.
[7]	Magnet Wire: 0.28 mm, Grade 2 ECW.
[8]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 6 mm Wide.
[9]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 9 mm Wide.
[10]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 12 mm Wide.
[11]	Bus Wire: #30 AWG.
[12]	Varnish: Dolph BC-359.

Table 5 - Transformer Materials List

9.5 Construction

Winding Preparation	Place the bobbin on the mandrel with the pin side to the right. Winding direction is clockwise i.e. top side moving away from operator.
WD1 ½ Primary	Start at pin 6, bring wires across through slot between pins 5 and 6. Close wind 12 turns, 2 strands of wire Item [6] in 1 layer with tight tension to fill the bobbin width in a neat flat wind.
Insulation	Use 1/2 turn of tape, Item [9], to hold winding in place. Bend end of winding across to exit in slot between Pins 4 and 5. Complete the 1½ turns of tape to secure the Primary 1 winding end in place. Terminate wind on pin 4.
WD2 Primary Bias	Start at pin 1, bring wire across through slot between pins 1 and 2. Close wind 3 turns, single strand Item [7] with tight tension. Take wire through slot between pins 1 and 2 and terminate on pin 2.
WD3 Screen 1	Take 3 strands of Item [7], each 750 mm long. Lay the ends of the strands next to WD2 and secure with a small piece of tape as shown. Carefully wind 8 turns tri-filar winding, close wound tight tension, being careful not to pull the free ends out of their securing tape.
Insulation	Use 1/2 turn of tape, Item [9], to hold winding in place. Bend end of winding across to exit in slot between pins 2 and 3. Complete the 1½ turns of tape to secure the Screen 1 winding end in place. Terminate the winding on pin 3
WD4 LED Secondary	Start at pin 7, bring the wire across through slot between pins 7 and 8. Close wind 9 turns, single strand of wire Item [4] in 1 layer with tight tension to fill the bobbin width in a neat flat wind. Cut to leave 5cm of free wire and secure it to the mandrel chuck with tape
Insulation	Secure wind in place with 1½ turns of tape Item [9].
WD5 Unregulated CV2 (Secondary bias wind)	Start winding on pin 10, bring wire across through slot between pins 10 and 11. Wind 1 turn, single strand of Item [5]. Bring back through slot between pins 10 and 11 and terminate on pin 11.
WD6 CV1 Secondary	Take 3 x 24cm lengths of Item [3]. Start 2 strands on pin 12 and the 3rd strand on pin 11. Pins 11 and 12 are connected together via the PCB. Take across through slot between pins 11 and 12. Wind 2 turns tri-filar and secure the ends to the mandrel

	chuck for termination later.
Insulation	Secure winding with 1 ½ layers of tape Item [9]
WD7 Screen 2 and 3	Take 2 stands of Item [7] 125 cm long and temporarily secure to pin 3. Take across through the slot between pins 2 and 3. Wind 14 turns bi-filar, close winding and tight tension as neatly as possible.
Termination and insulation of Screens 2and3	Secure with ½ turn of tape Item [9]. Determine which ends belong to Screen 2 and Screen 3. A multimeter, different colored strands or labelling would be helpful. Terminate Screen 2 'START' and Screen 3 'FINISH' to pin 3. Cut Screen 2 'FINISH' and Screen 3 'START' to make unconnected buried ends. Ensure the bare ends cannot touch. Complete 1½ turns of tape to secure ends in place. By reference to the Winding Stack Diagram it can be seen that Screens 2 and 3 form 2 counter wound coils and will approximately emulate an equi-potential screen such as a copper foil screen, hence the particular instructions for this winding.
WD8 Primary 2 2nd ½ Primary	Start at pin 4 and bring wires across through slot between pins 4 and 5. Close wind 12 turns, 2 strands of wire Item [6] in 1 layer with tight tension to fill the bobbin width in a neat flat wind as possible.
Insulation	Secure wind with 1 layer of tape Item [9]. Take wind ends across the bobbin and through the slot between pins 3 and 4. Complete the 1½ turns of tape to secure.
Termination	Bring the Primary 2 ends back up and pass through the slot between pins 4 and 5 and terminate at pin 5.
Termination and insulation CV1 Secondary wind	Bend down the ends of CV1 and LED secondaries and secure with 2 turns of tape, Item [9]. Take the 3 ends of CV1 secondary winding and pass through the slot between pins 8 and 9 and terminate 2 ends on pin 9 and 1 end on pin 8. Pins 8 and 9 are connected together via the PCB. Take the end of the LED secondary winding through the slot between pins 10 and 11 and terminate on pin 11.
Gap Core	Gap core to 285 μH ±5%

Table 6 - Transformer Construction Instructions

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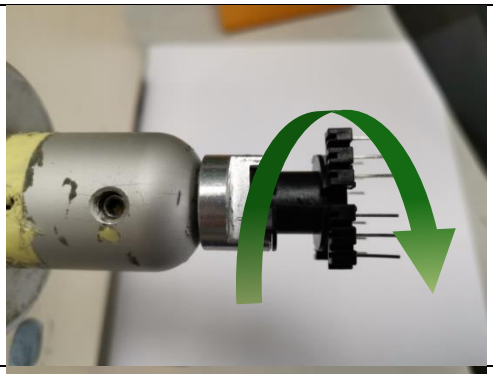
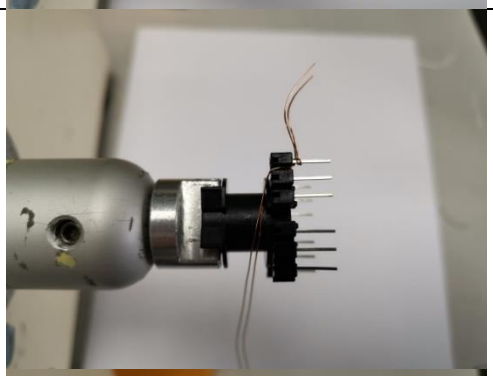
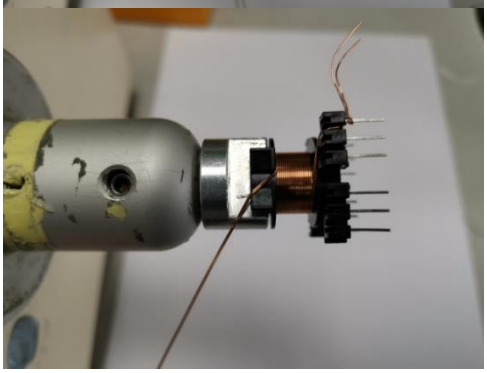
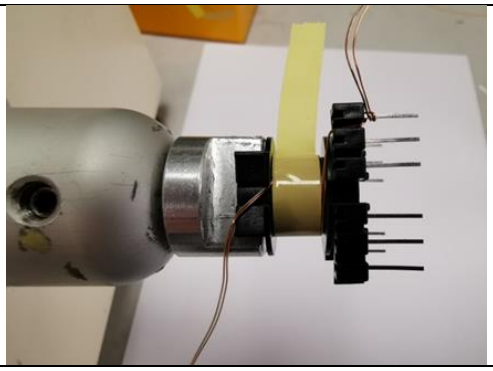
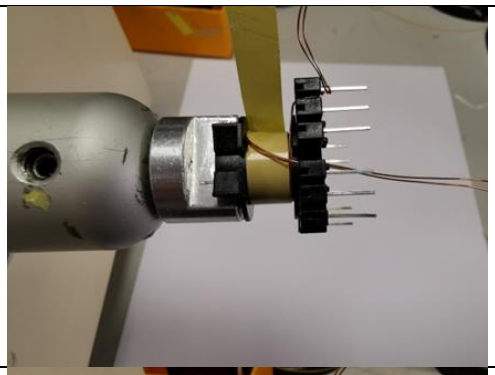
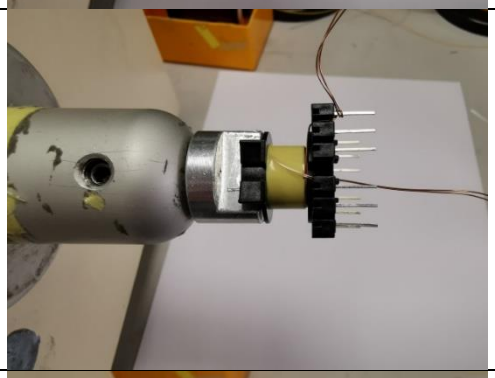
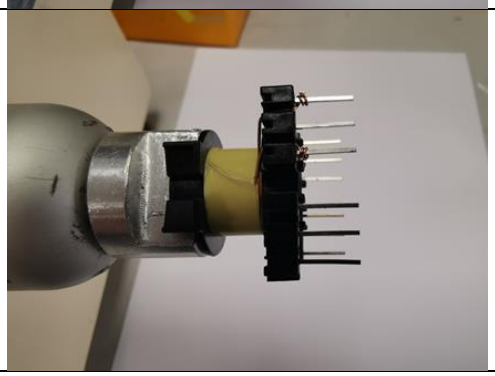
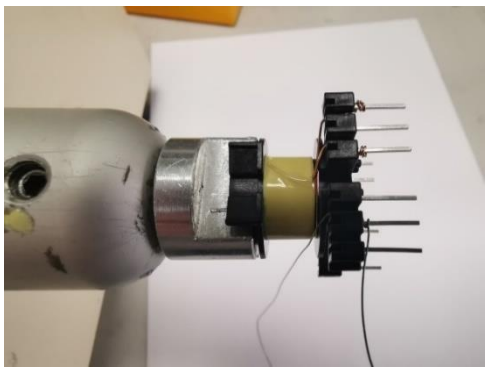
9.6 Winding Illustration

N.B. a bobbin without the extended skirt has been used in these photographs to improve termination visibility.

Winding Preparation		Place the bobbin on the mandrel with the pin side to the right. Winding direction is in the clockwise direction i.e. top side moving away from operator.
WD1 **Primary 1** **½ Primary**	 	Start at pin 6, bring wires across through slot between pins 5 and 6. Close wind 12 turns, 2 strands of wire Item [6] in 1 layer with tight tension to fill the bobbin width in a neat flat wind.
Insulation layer		Use 1/2 turn of tape, Item [9], to hold winding in place.

		Bend end of winding across to exit in slot between pins 4 and 5.
		Complete the 1½ turns of tape to secure the Primary 1 winding end in place.
		Terminate wind on pin 4.
WD2 **Primary Bias Wind**		Start at pin 1, bring wire across through slot between pins 1 and 2. Close wind 3 turns, single strand Item [7] with tight tension.

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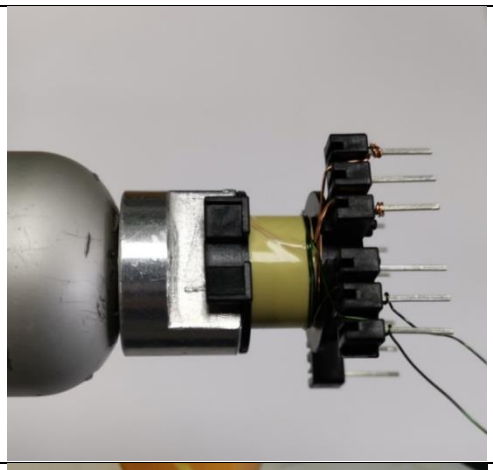
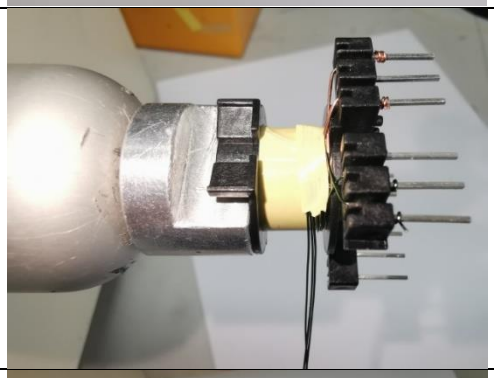
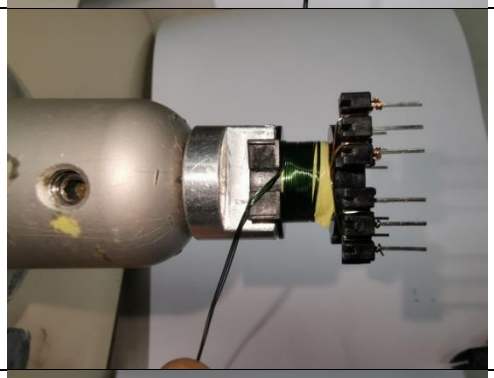
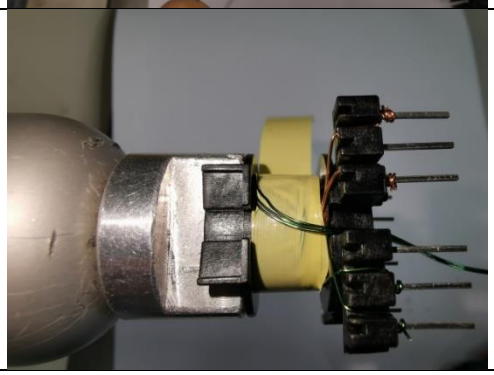
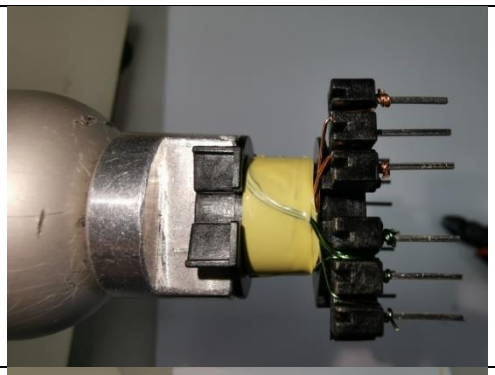
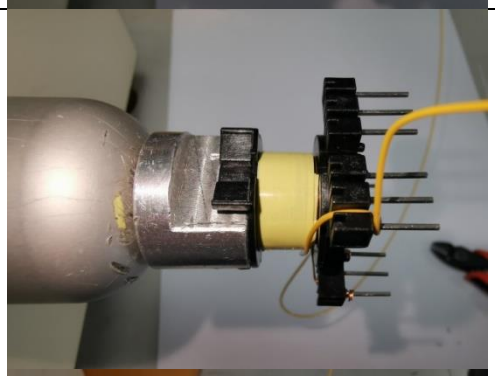
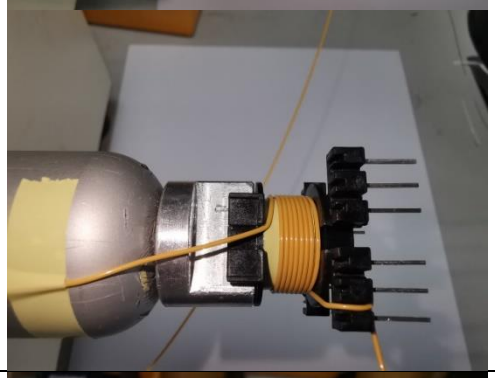
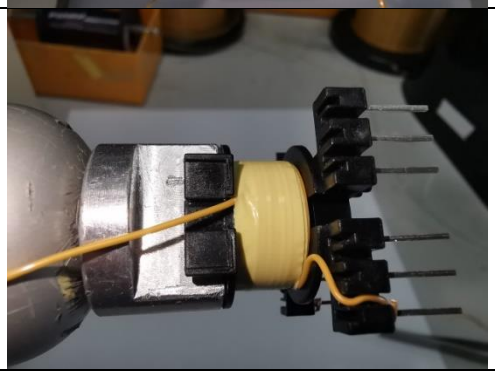
		Take wire through slot between pins 1 and 2 and terminate on pin 2.
WD3 **Screen Winding 1**		Take 3 strands of Item [7], each 750 mm long. Lay the ends of the strands next to WD2 and secure with a small piece of tape as shown.
		Carefully wind 8 turns tri-filar winding, close wound tight tension, being careful not to pull the free ends out of their securing tape.
		Use 1/2 turn of tape, Item [9], to hold winding in place. Bend end of winding across to exit in slot between pins 2 and 3.

		Complete the 1½ turns of tape to secure the Screen 1 winding end in place. Terminate the winding on pin 3
WD4 **LED Secondary wind**	 	Start at pin 7, bring the wire across through slot between pins 7 and 8. Close wind 9 turns, single strands of wire Item [4] in 1 layer with tight tension to fill the bobbin width in a neat flat wind. Cut to leave 5 cm of free wire and secure it to the mandrel chuck with tape
Insulation		Secure wind in place with 1 ½ turns of tape Item [9].

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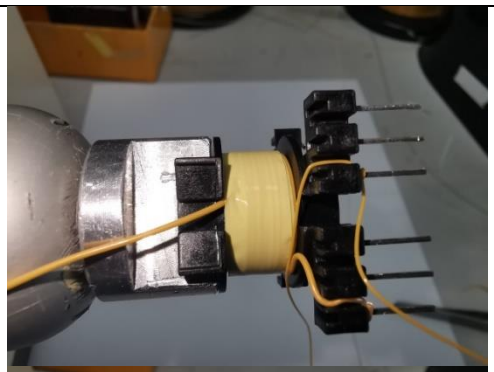
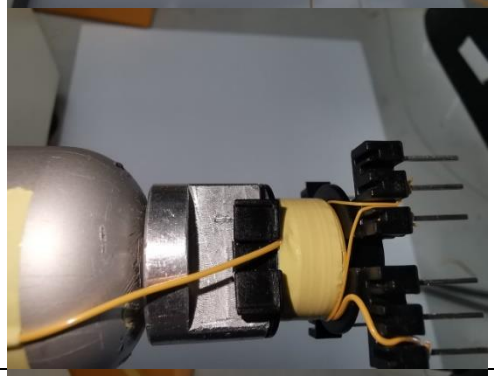
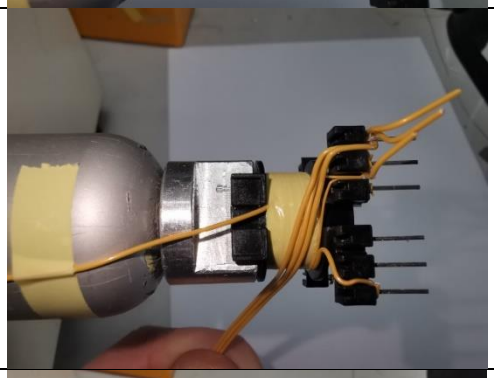
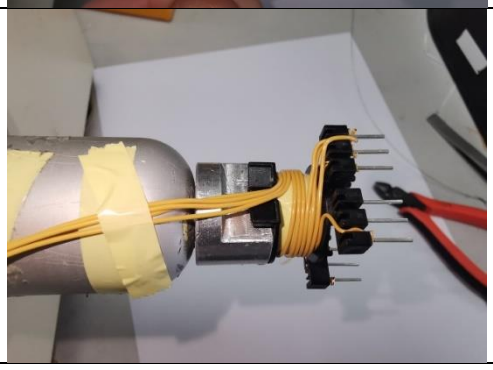
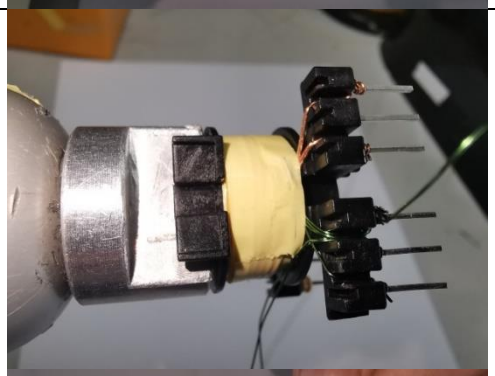
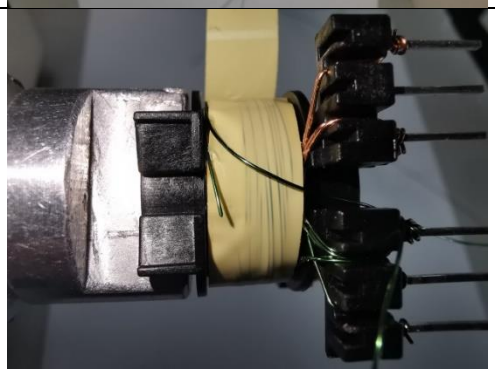
WD5 **Unregulated CV2** **(Secondary bias wind)**		Start winding on pin 10, bring wire across through slot between pins 10 and 11. Wind 1 turn, single strand of Item [5].
		Bring back through slot between pins 10 and 11 and terminate on pin 11.
WD6 **CV1 Secondary Winding**		Take 3 x 24 cm lengths of Item [3]. Start 2 strands on pin 12 and the 3rd strand on pin 11. Pins 11 and 12 are connected together via the PCB. Take across through slot between pins 11 and 12.
		Wind 2 turns tri-filar and secure the ends to the mandrel chuck for termination later.

Insulation		Secure winding with 1 ½ layers of tape Item [9]
WD7 **Screen 2+3**	 	Take 2 stands of Item [7] 125 cm long and temporarily secure to pin 3. Take across through the slot between pins 2 and 3. Wind 14 turns bi-filar, close winding and tight tension as neatly as possible.
		Secure with ½ turn of tape Item [9]. Determine which ends belong to Screen 2 and Screen 3. A multimeter, different colored strands or labelling would be helpful. Terminate Screen 2 'START' and Screen 3 'FINISH' to pin 3. Cut Screen 2 'FINISH' and Screen 3 'START' to make unconnected buried ends. Ensure the bare ends cannot touch. Complete 1½ turns of tape to secure ends in place.

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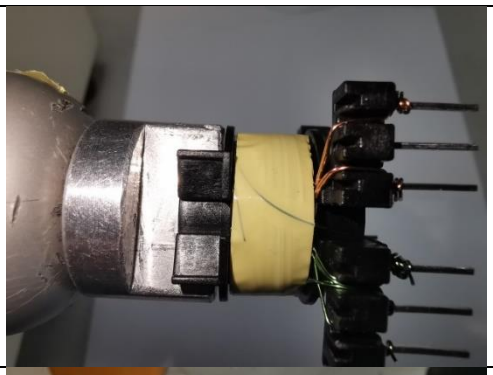
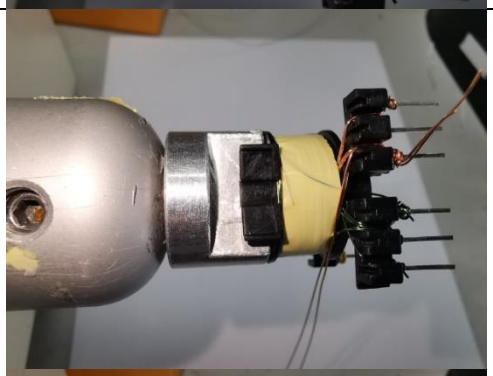
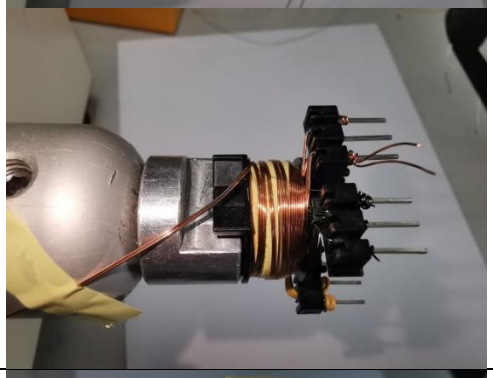
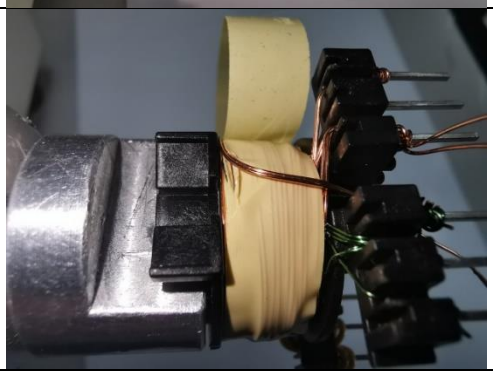
		By reference to the Winding Stack Diagram it can be seen that Screens 2 and 3 form 2 counter wound coils and will approximately emulate an equi-potential screen such as a copper foil screen, hence the particular instructions for this winding.
WD8 **Primary 2** **2nd ½ primary**	 	Start at pin 4 and bring wires across through slot between pins 4 and 5. Close wind 12 turns, 2 strands of wire Item [6] in 1 layer with tight tension to fill the bobbin width in a neat flat wind as possible.
		Secure wind with 1 layer of tape Item [9]. Take wind ends across the bobbin and through the slot between pins 3 and 4. Complete the 1½ turns of tape to secure.

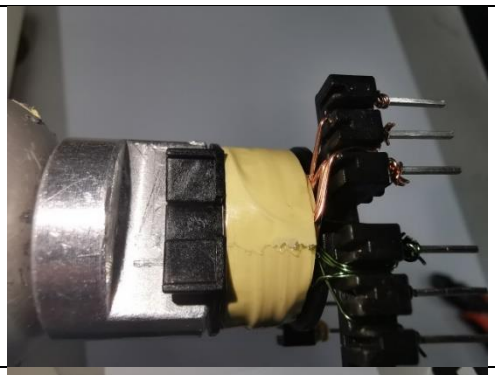
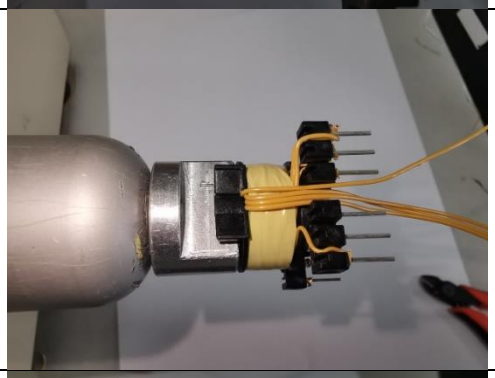
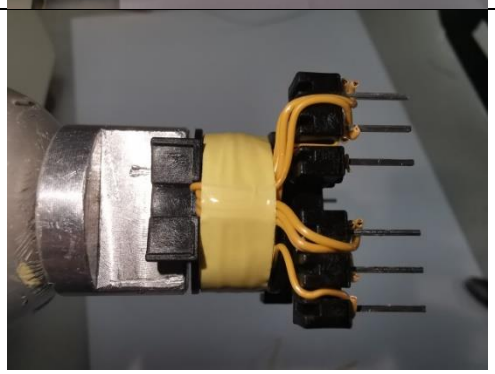
		Bring the Primary 2 ends back up and pass through the slot between pins 4 and 5 and terminate at pin 5.
Terminating CV1 Secondary Winding		Bend down the ends of CV1 and LED secondaries and secure with 2 turns of tape, Item [9].
		Take the 3 ends of CV1 secondary winding and pass through the slot between pins 8 and 9 and terminate 2 ends on pin 9 and 1 end on pin 8. Pins 8 and 9 are connected together via the PCB. Take the end of the LED secondary winding through the slot between pins 10 and 11 and terminate on pin 11. Gap core to achieve 285 μH.

Table 7 - Transformer Winding Illustrations

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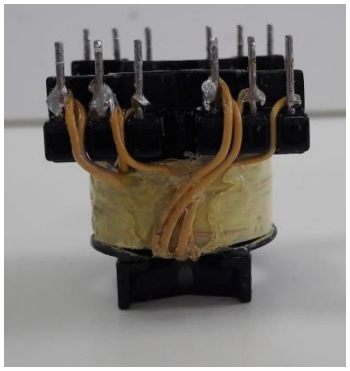
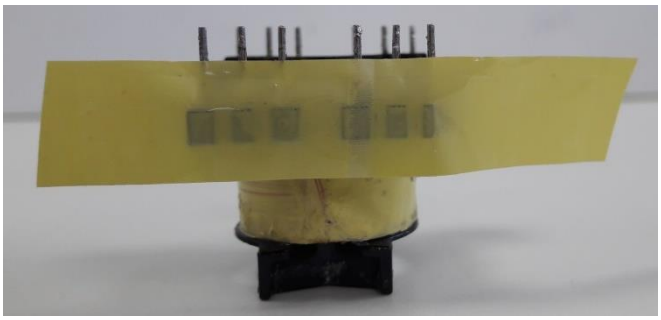
10 Improvement of Voltage Isolation from Core to Pins 7 and 12

These preparations are to improve ESD and surge performance of the transformer. Ideally a bobbin with an extended secondary molding to the pins should be used, or flying leads on the secondaries.

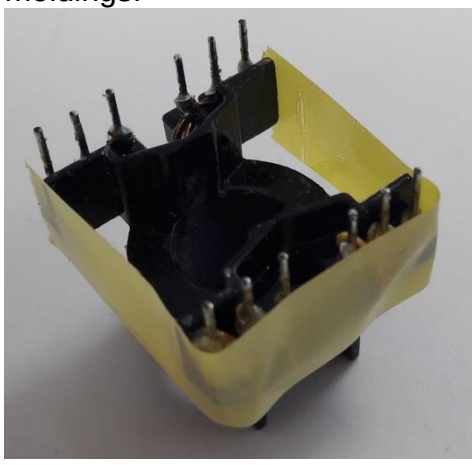
N.B. This bobbin has the extended skirt for accuracy of instructions.

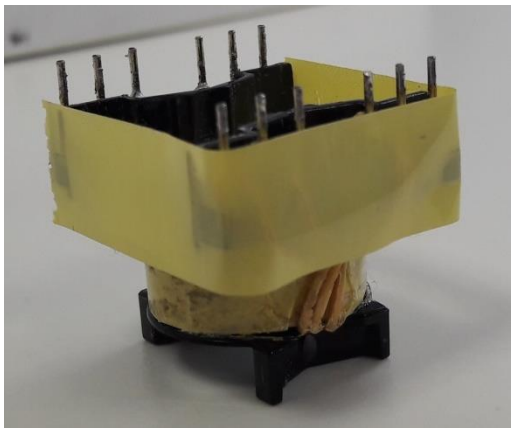
- Once windings complete, cut a piece of 7 cm x 12 mm tape Item [10] and apply as shown, to secondary side edge. The top edge of the tape is to be at the same level as the extended bobbin skirt as shown.
-





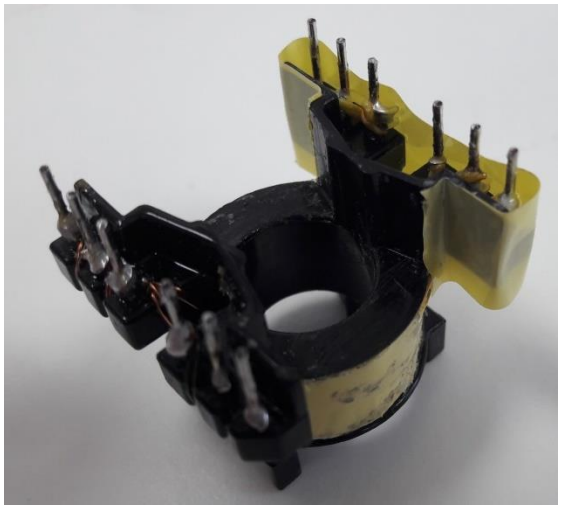
- Fold both sides over to stick to the sides of the secondary pin support moldings.



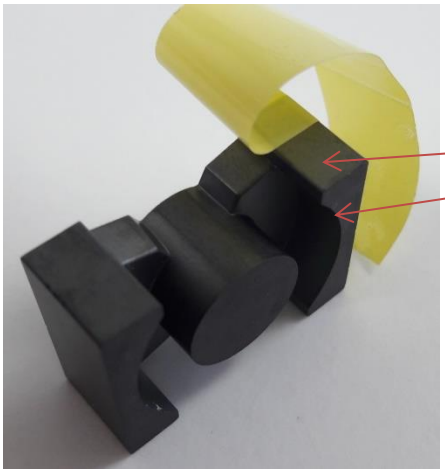


- With the back edge of a scalpel, push the tape to stick to the inner surfaces as shown, ensure the tape goes right up to the corners.

-
- With a sharp scalpel, trim both ends of the tape to be flush with the outside corner of the bobbin as shown.



- Cut a piece of 6cm x 12mm tape Item [10] and apply it side surface of the core half way along as shown. The edge of the tape is to be level with the inside edge of the bottom of the core as shown.



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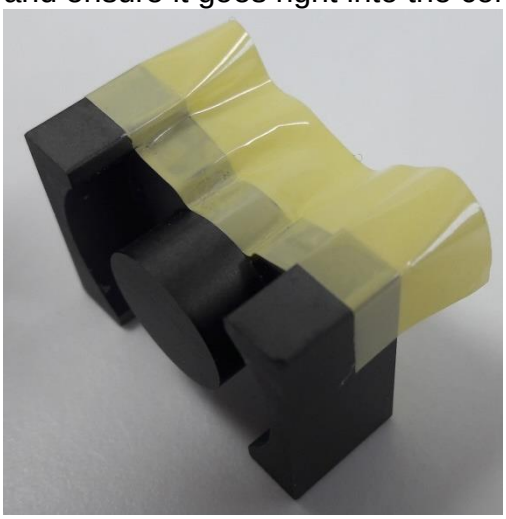
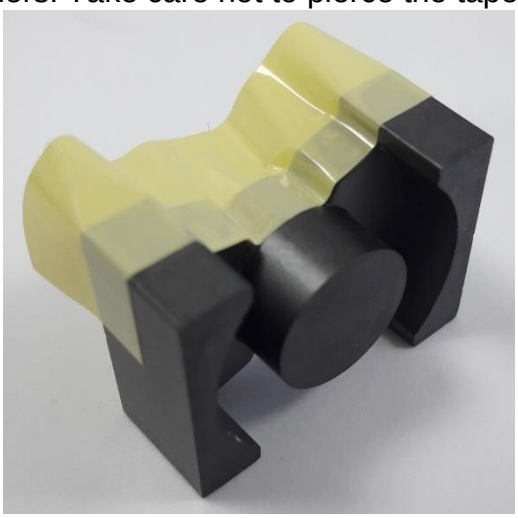
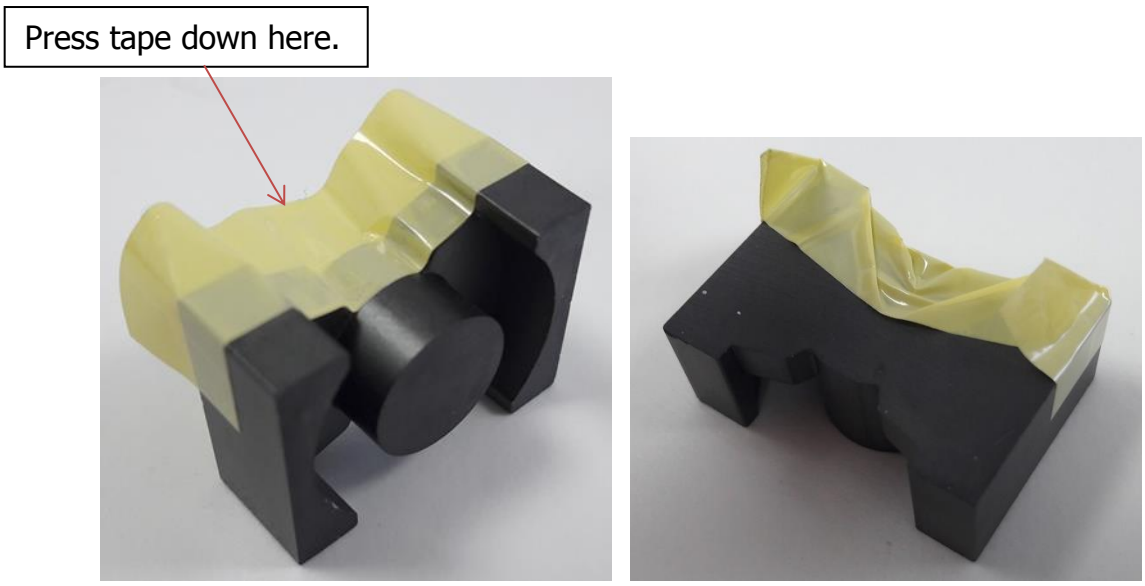
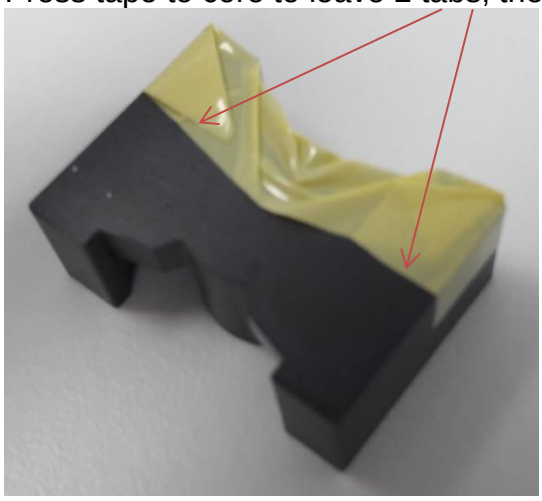
- With the back edge of a scalpel or similar, push the tape to the core surface and ensure it goes right into the corners. Take care not to pierce the tape.

- Press the centre of the free tape and push it down to stick to the core.



- Press tape to core to leave 2 tabs, then fold and stick those tabs down.



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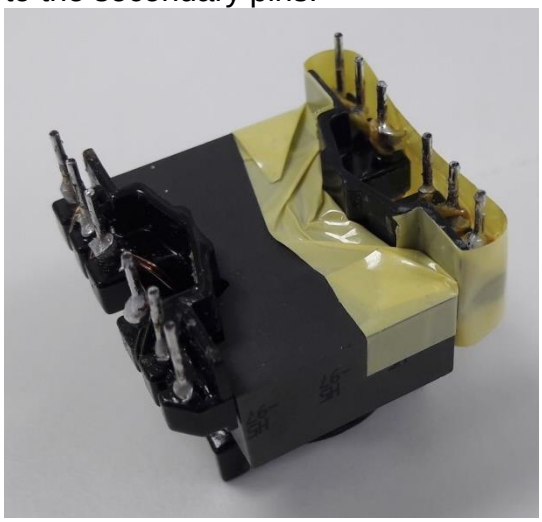
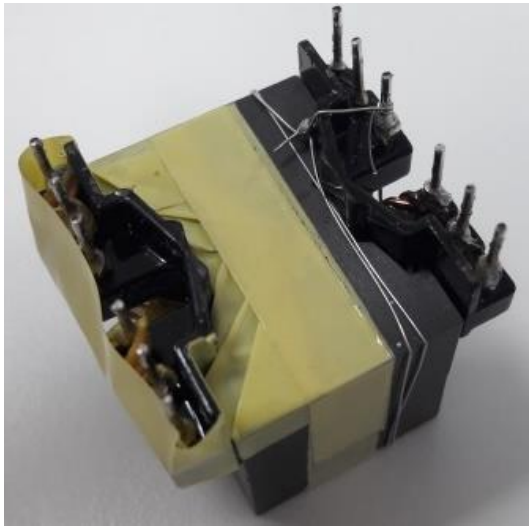
- Insert insulated core half into the underside of the bobbin with the tape next to the secondary pins.



- Insert top core half and secure with 2 layers of tightly wound 6 mm tape Item [8].

- Solder a 200 mm length of #30 AWG tinned copper wire to pin 3, leading towards the core.
- Where it reaches the core surface, bend at a right angle to the nearest corner edge then wind 2 turns tightly around the core.
- Solder wire end to wire going to pin 3 to secure.
- Secure the wire to the core with a length of tape Item [8].
- Varnish dip and cure in oven as required.



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3. Test

			Pins	CV (8-12)	LED (7-12)
L1	μH	285 ±5%	5 - 6	open	open
$L1_{S11}$		~18.24		short	open
$L1_{S12}$		~4.86		open	short
$L1_{S}$		~3.92		short	short

Table 8 - Transformer Parameter Measurements

Measured at 10 kHz, 0.5 $V_{RMS.}$

11 Performance Data

11.1 Efficiency

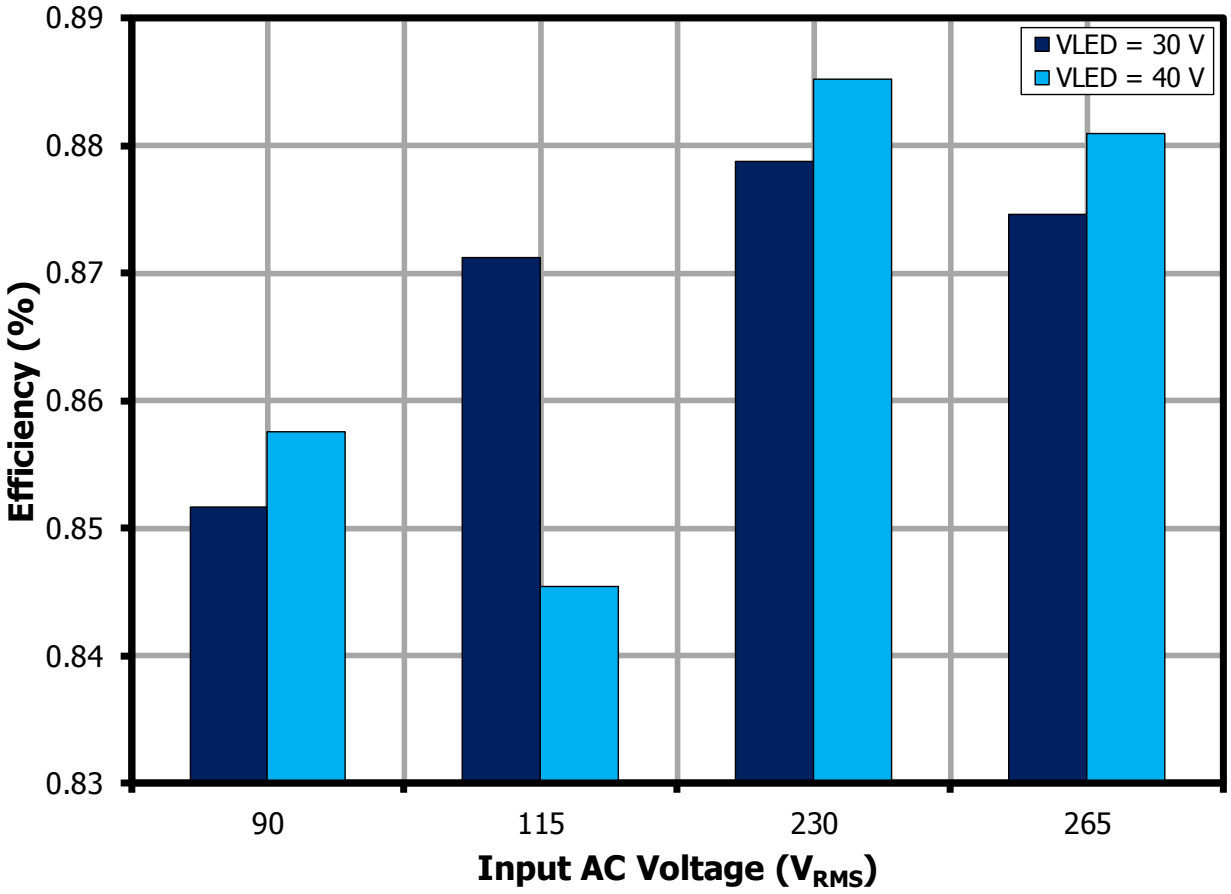

Figure 13 – Full Load (40 W) Efficiency vs. Line; Room Temperature

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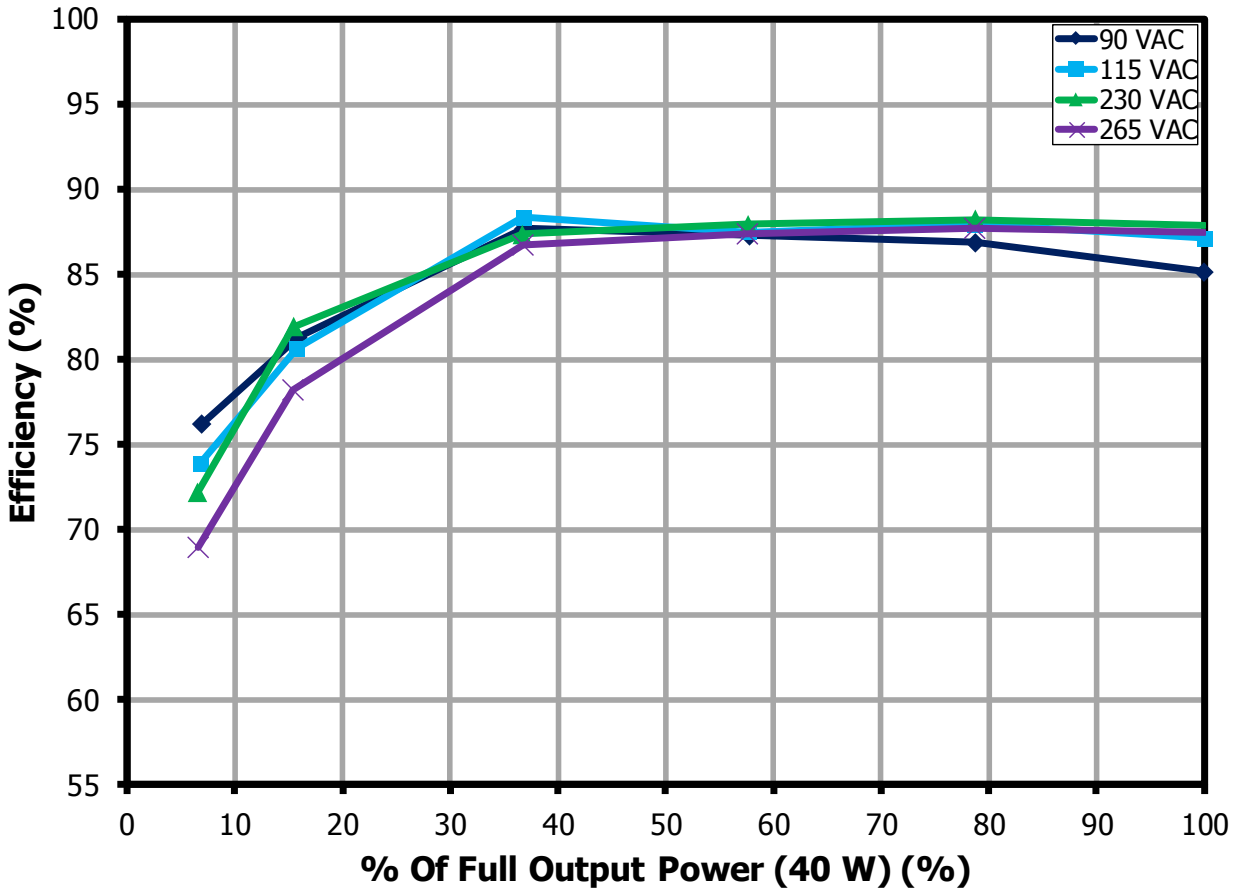

Figure 14 – Efficiency vs Output Power with 30 V LED Strings

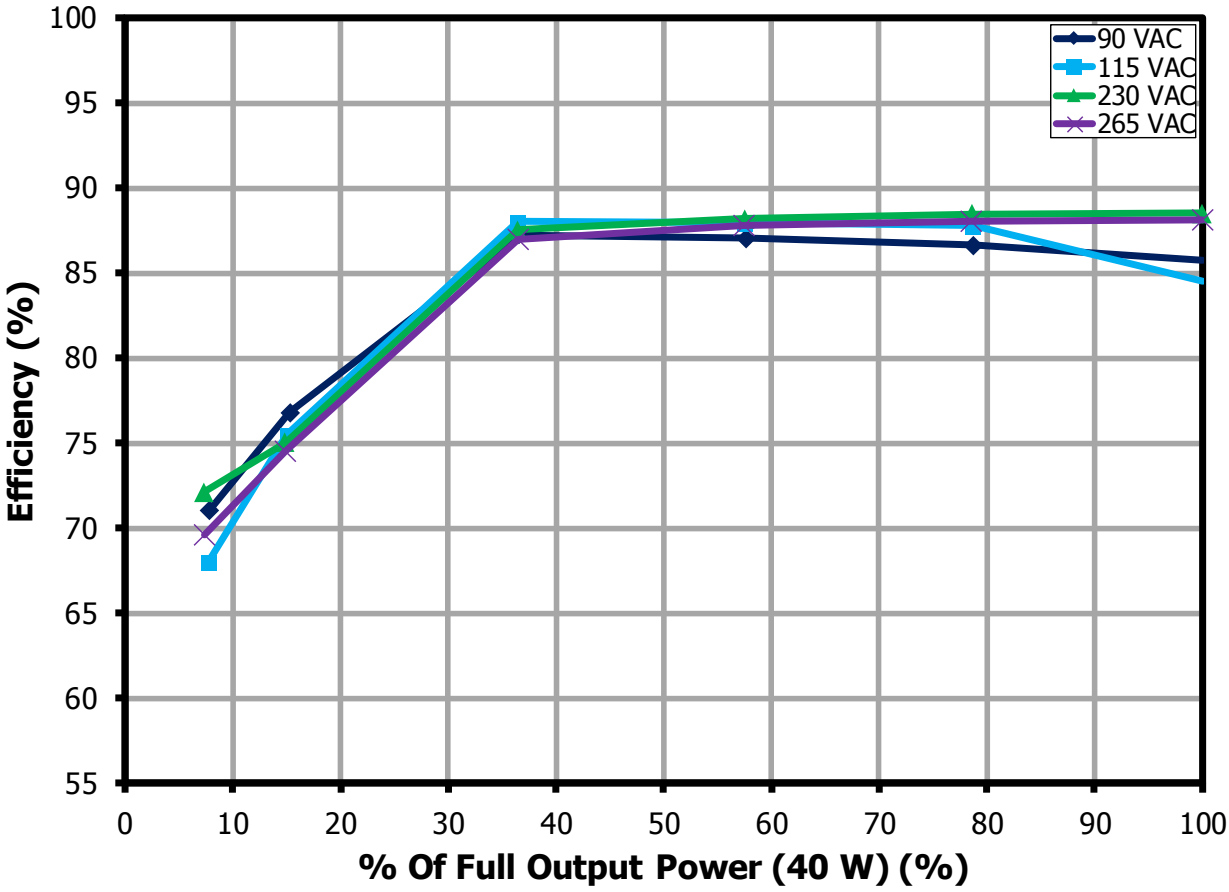

Figure 15 – Efficiency vs Output Power with 40 V LED Strings.

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11.2 CV1 Load Regulation and Cross-Regulation

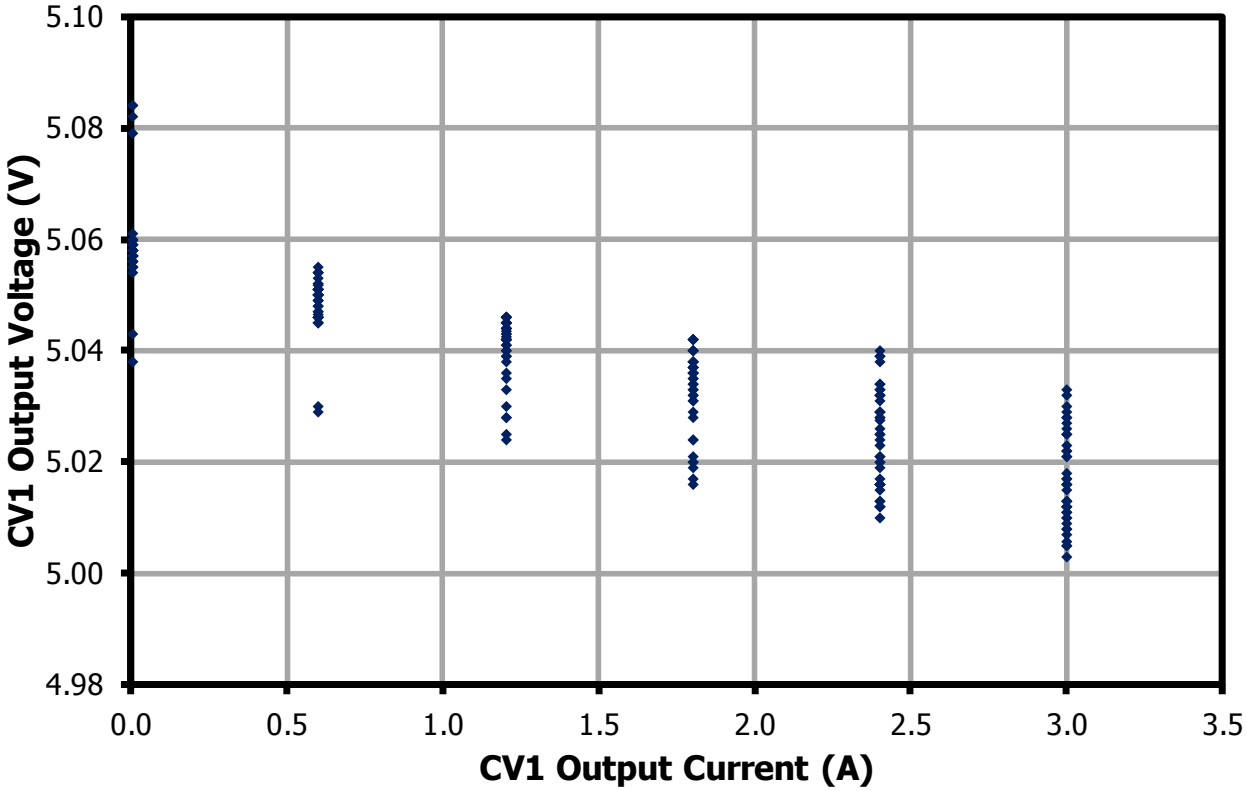

Figure 16 – CV1 Cross Regulation at All Conditions.

11.3 LED Current Cross Regulation with CV1 Load and VAC

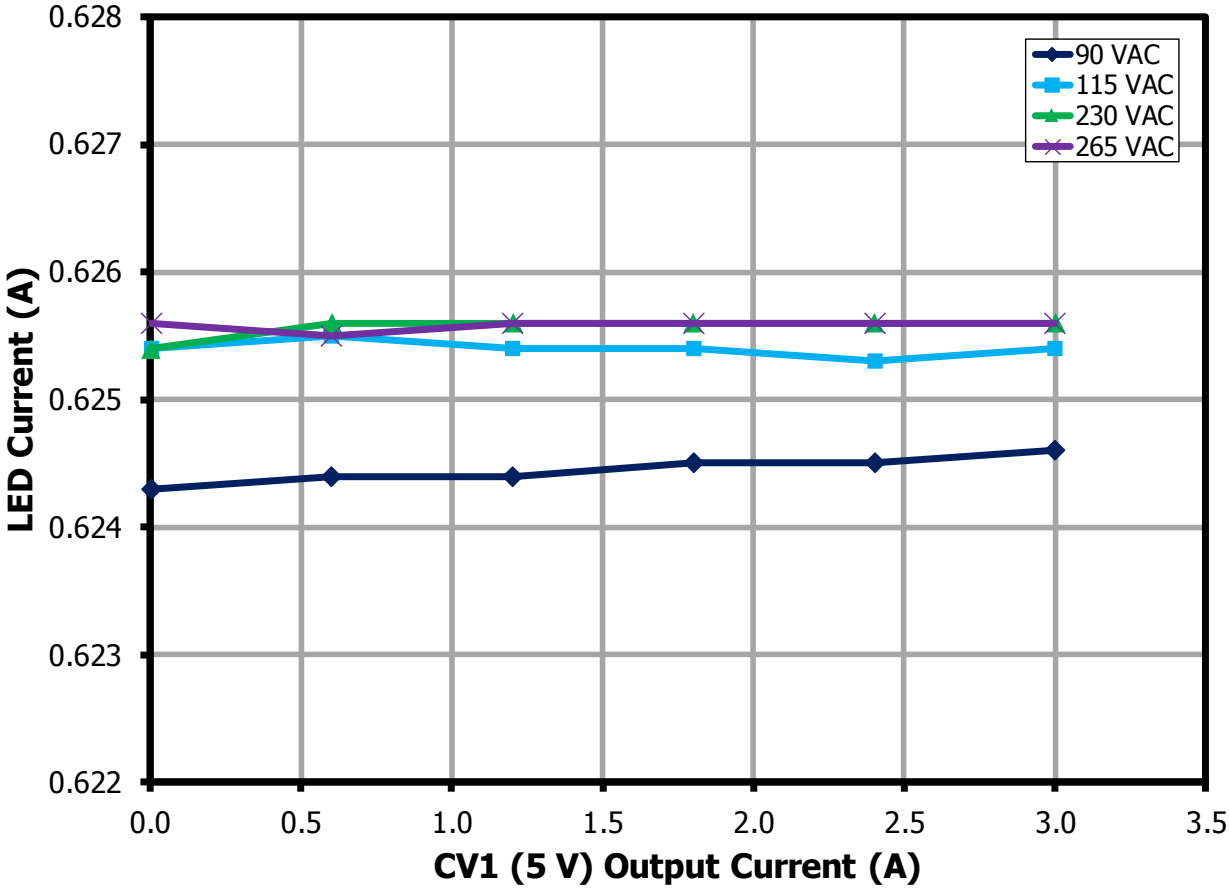

Figure 17 – Effect of CV1 Load and VAC Input on LED Current, 30 V LED Strings.

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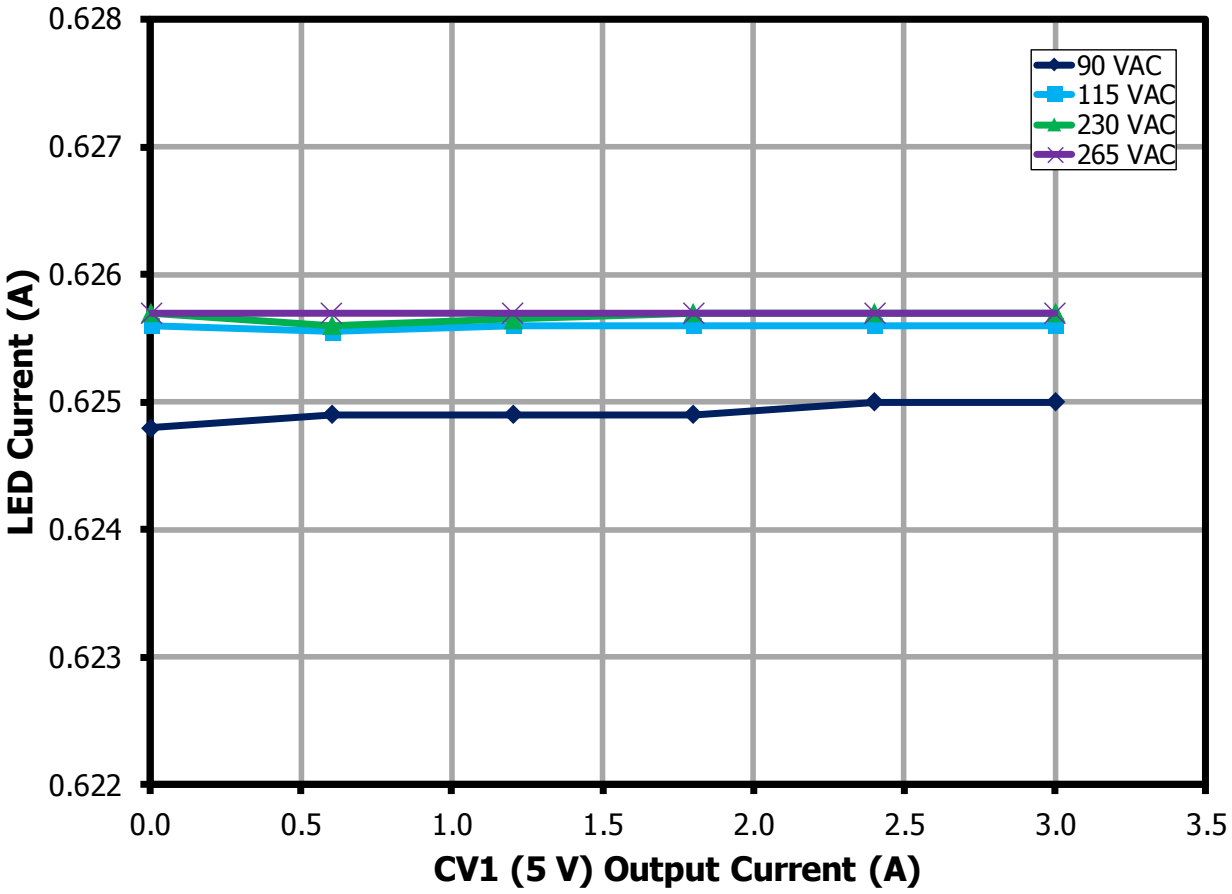

Figure 18 – Effect of CV1 Load and VAC Input on LED Current, 40 V LED Strings.

11.4 LED Dimming and String Current Matching

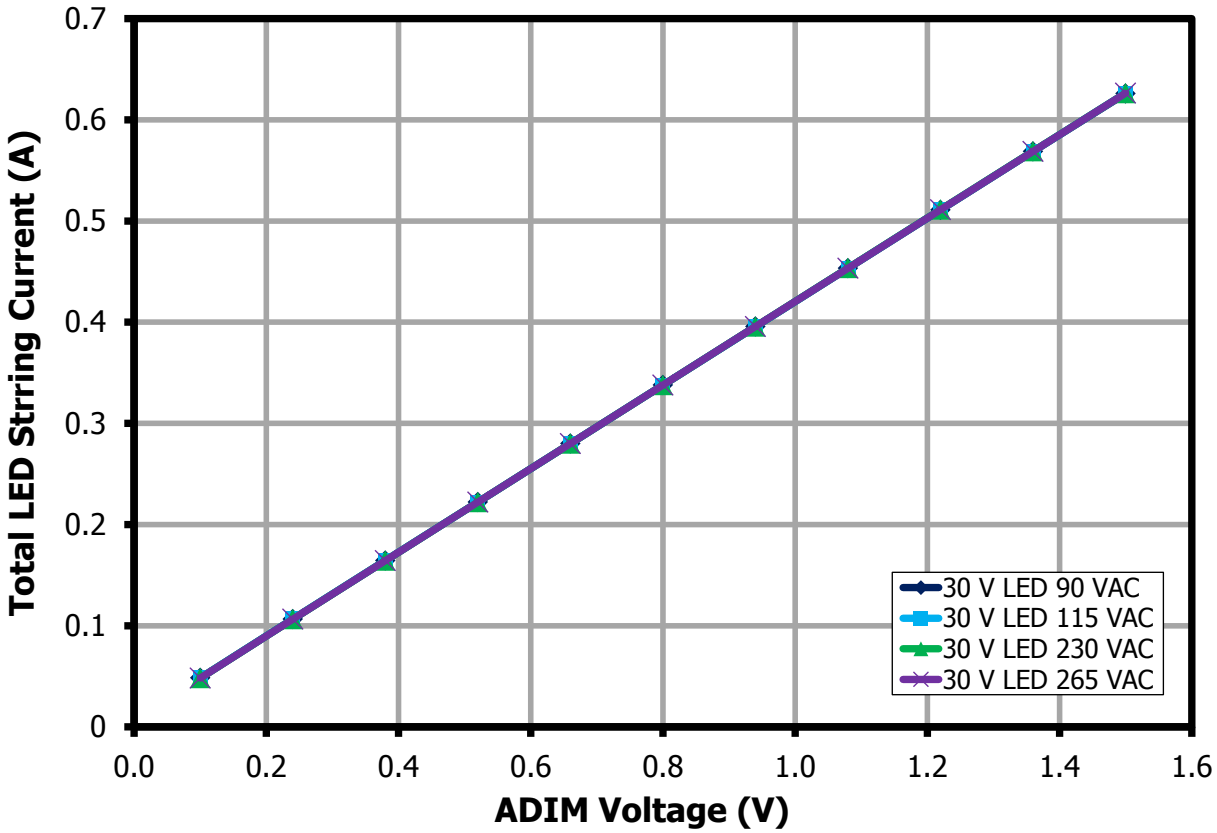

Figure 19 – Total LED Current vs. ADIM Input Voltage for 30 V LED Strings.

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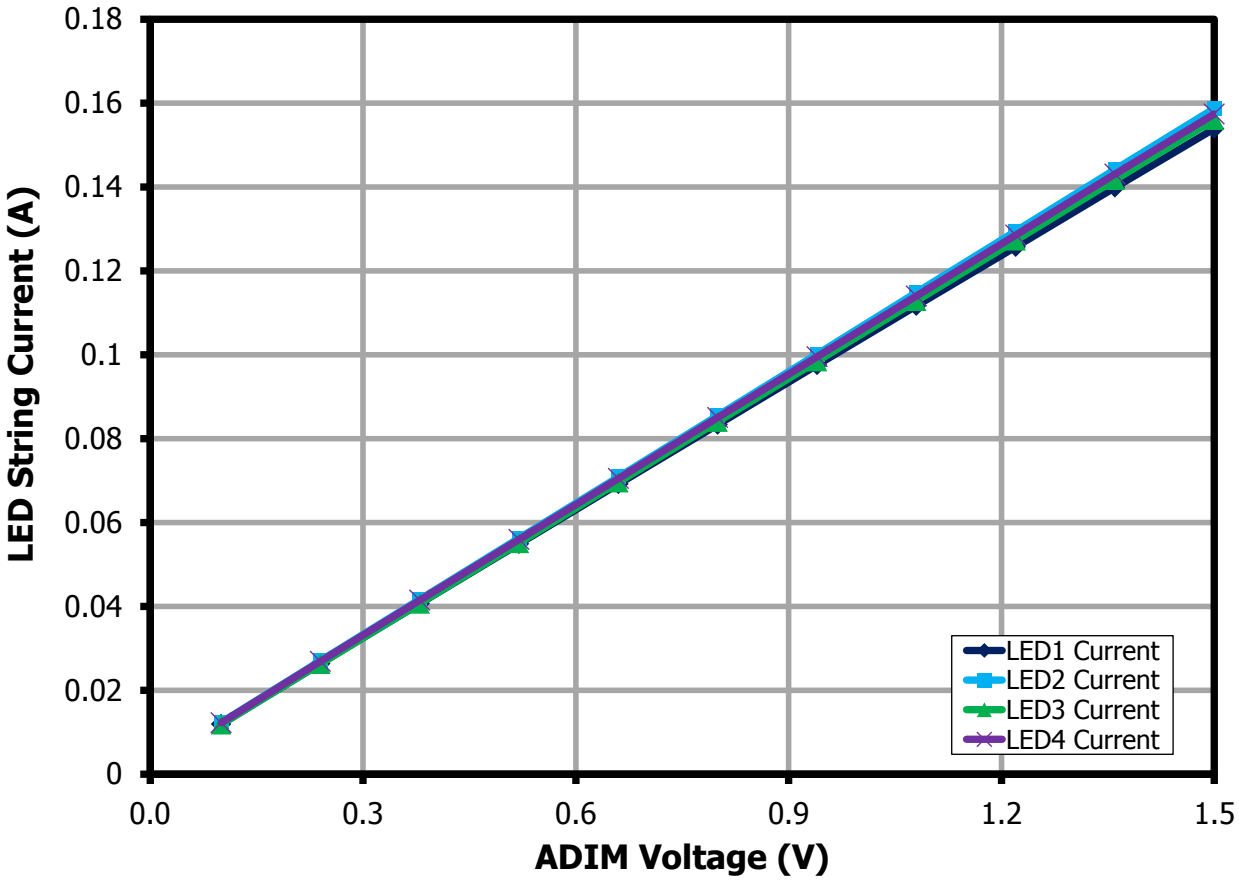

Figure 20 – 4 x 30 V String LED Current vs. ADIM Voltage at 90 VAC.

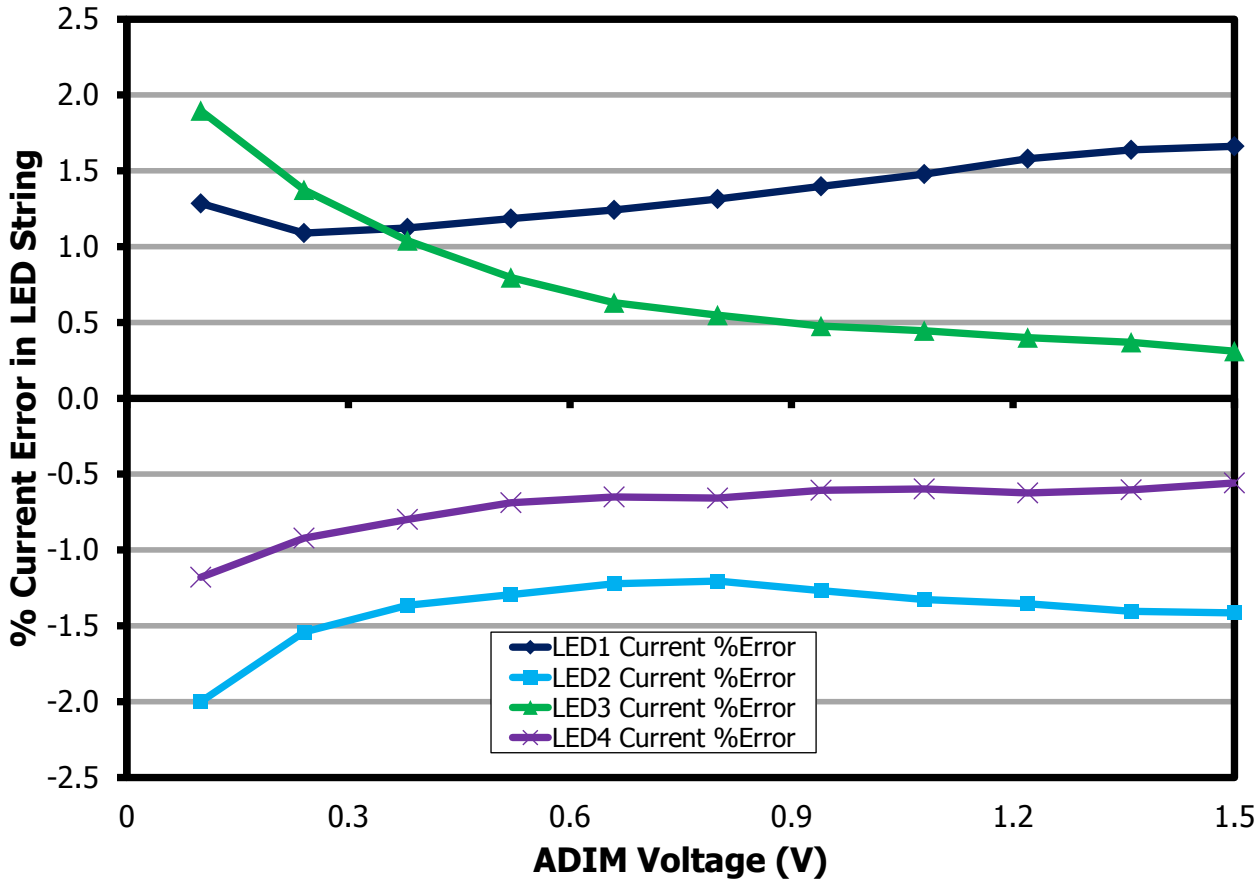

Figure 21 – LED String Current Matching Error for 30 V LED Strings at 90 VAC.

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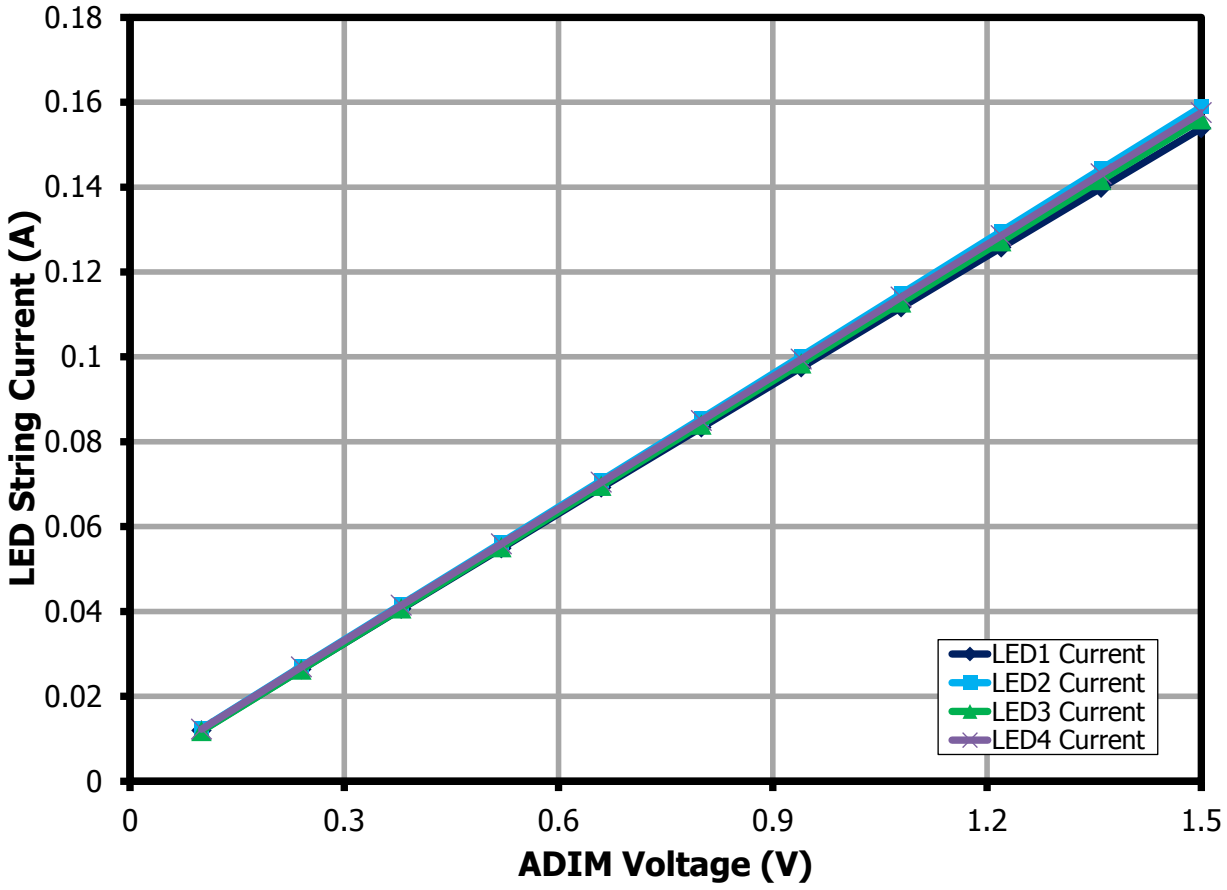

Figure 22 – 4 x 30 V String LED Current vs. ADIM Voltage at 115 VAC.

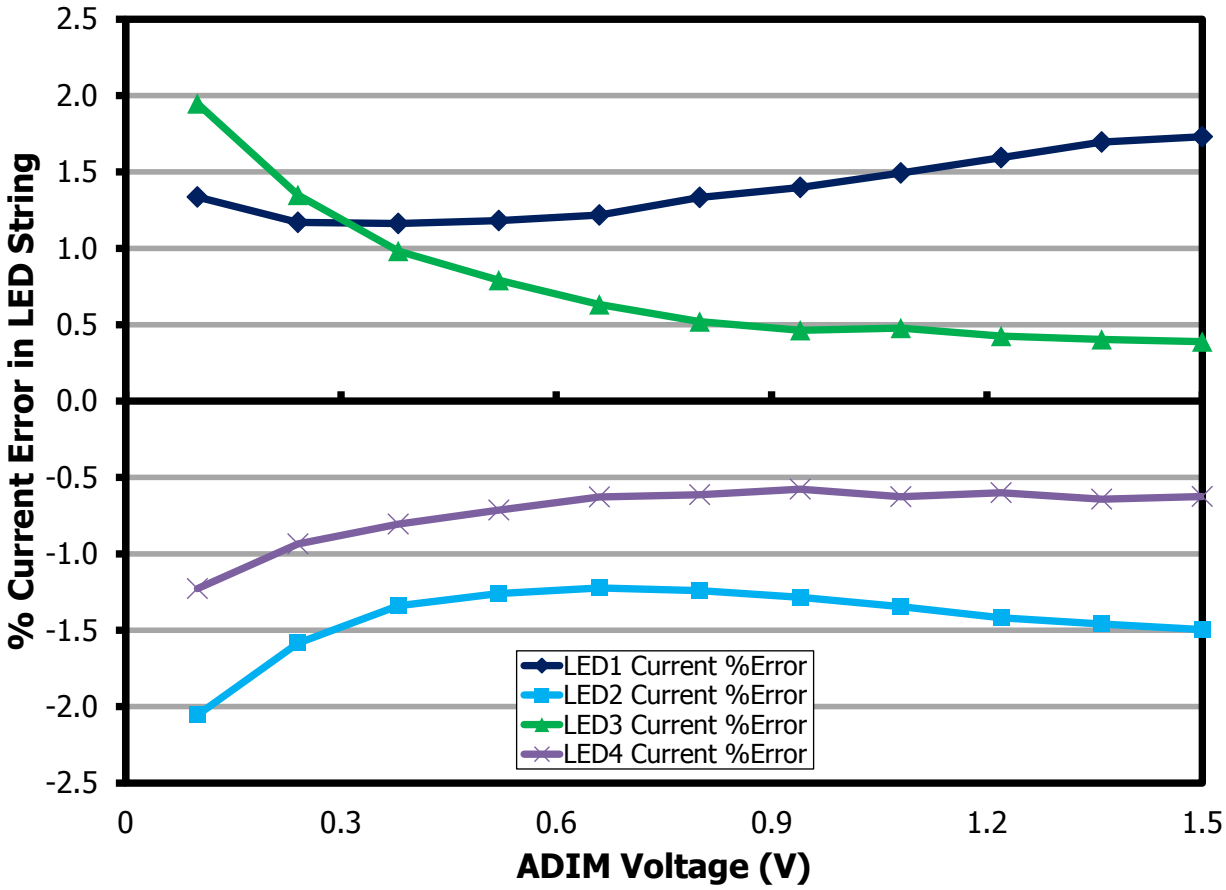

Figure 23 – LED String Current Matching Error for 30 V LED Strings at 115 VAC.

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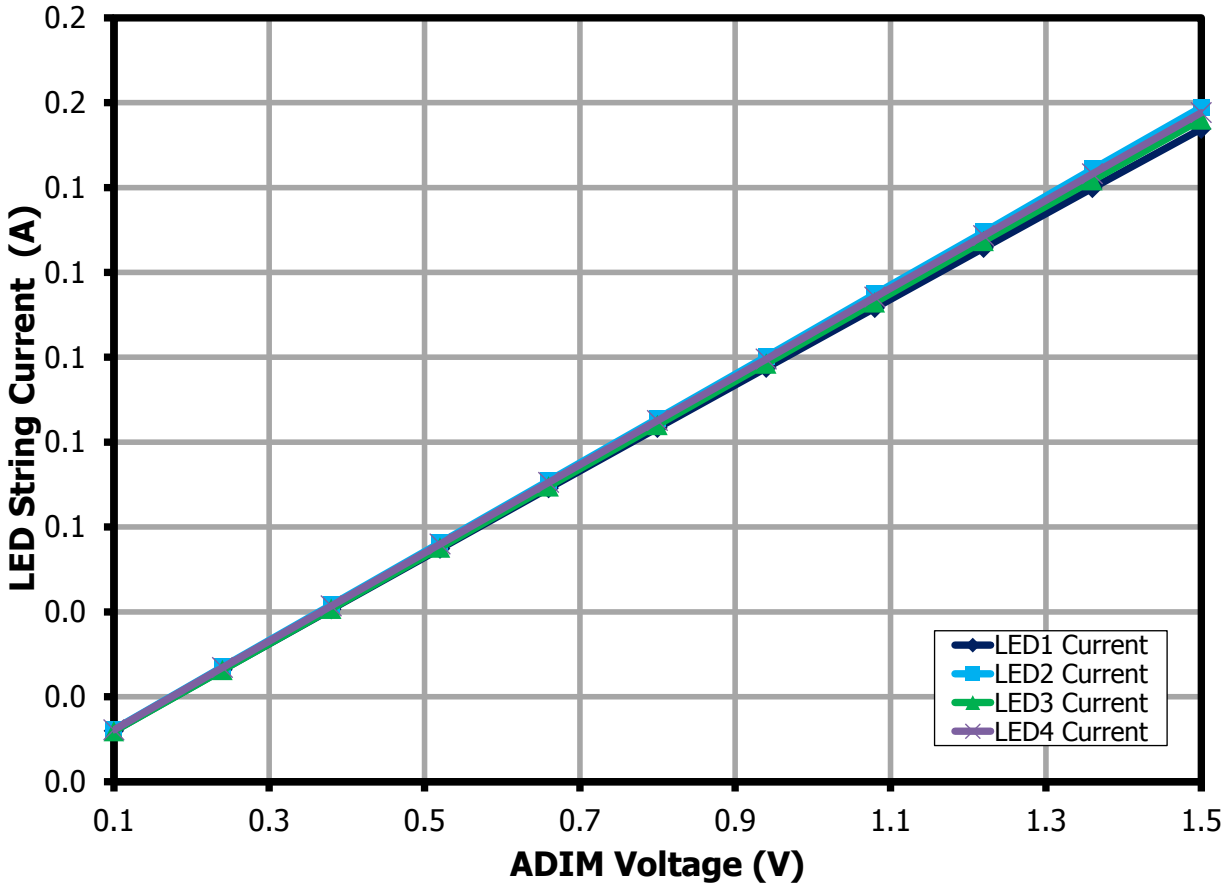

Figure 24 – 4 x 30 V String LED Current vs. ADIM Voltage at 230 VAC.

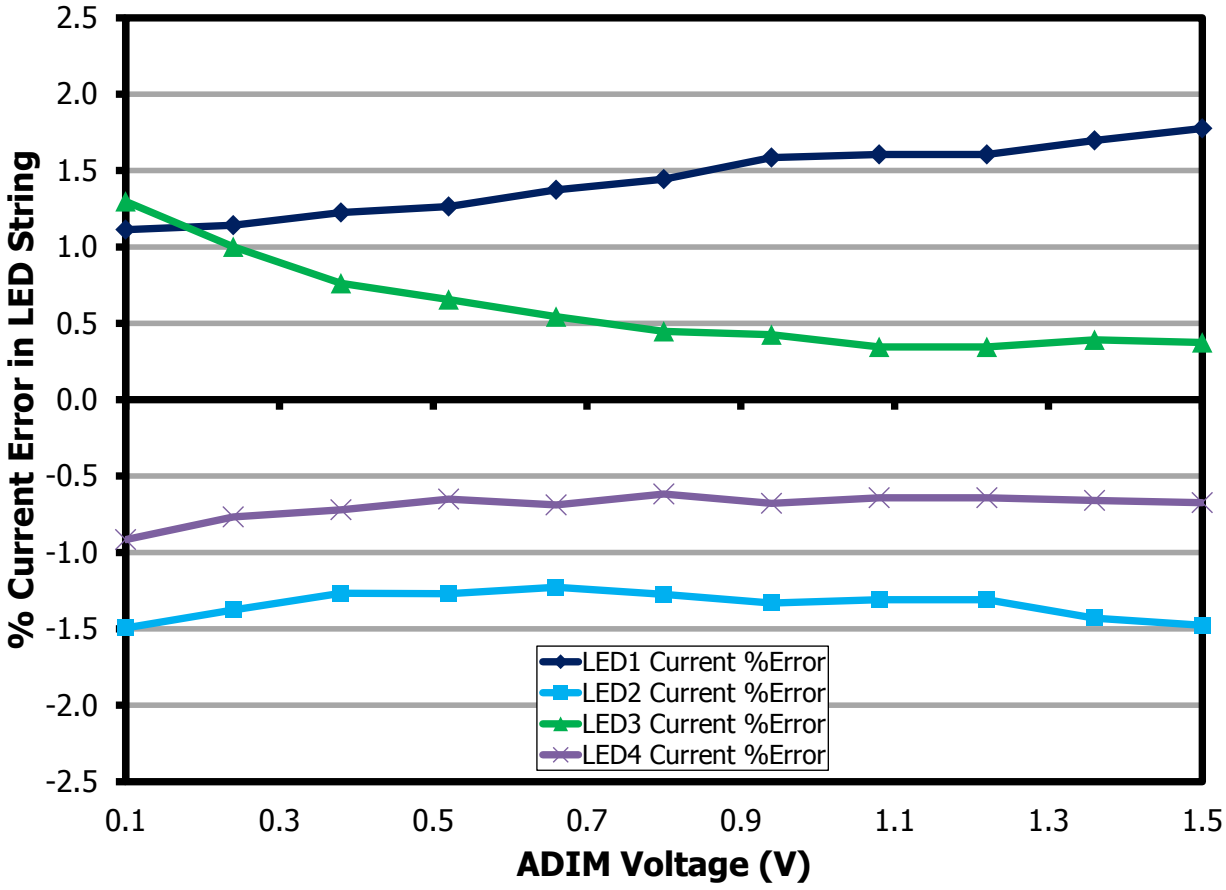

Figure 25 – LED String Current Matching Error for 30 V LED Strings at 230 VAC.

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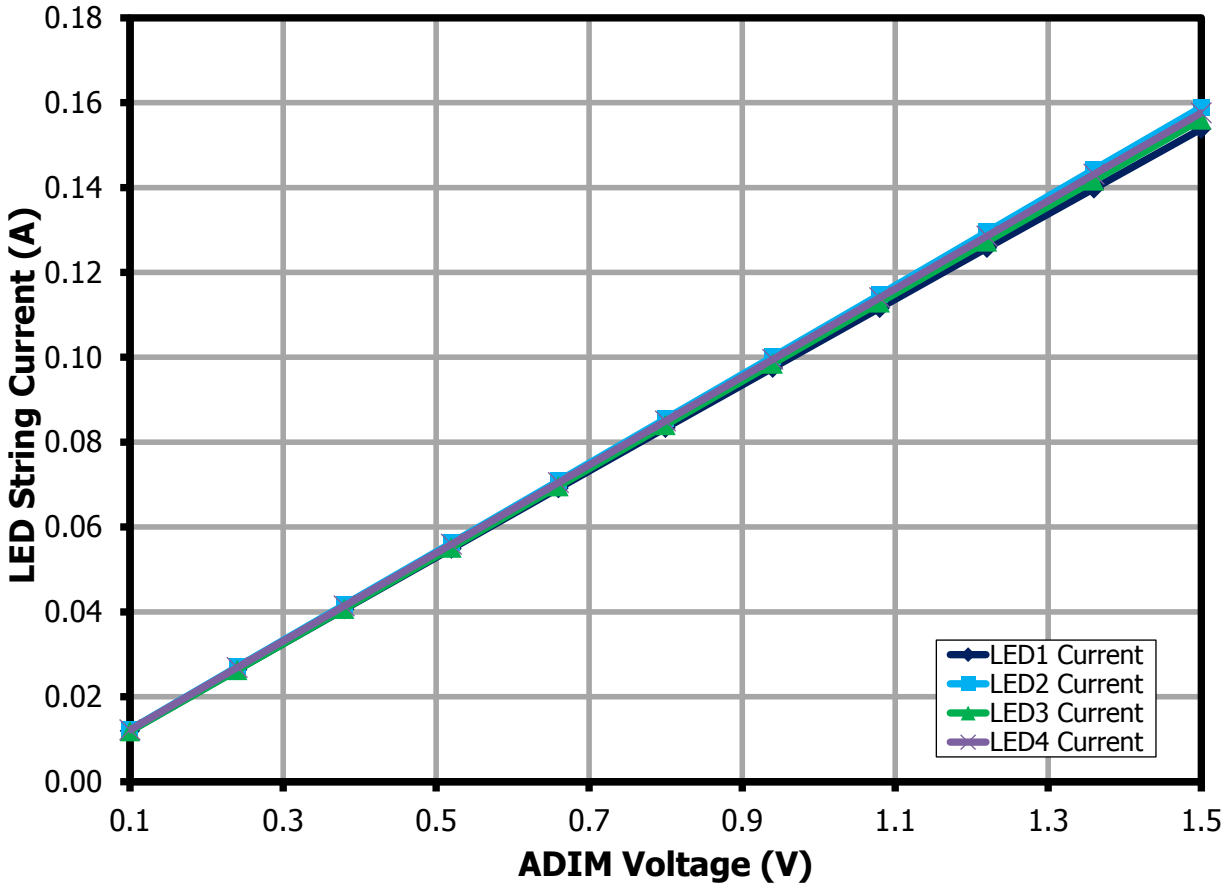

Figure 26 – 4 x 30 V String LED Current vs. ADIM Voltage at 265 VAC.

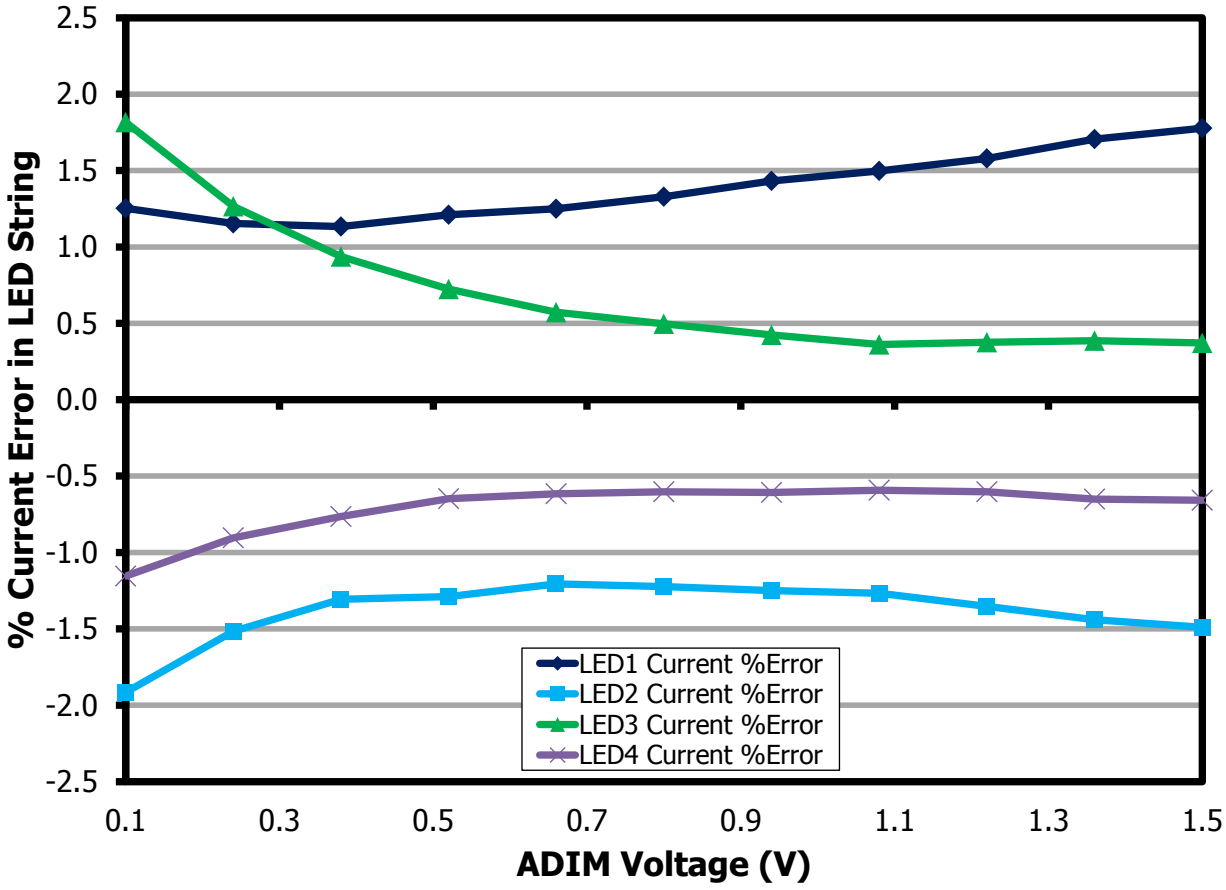

Figure 27 – LED String Current Matching Error for 30 V LED Strings at 265 VAC.

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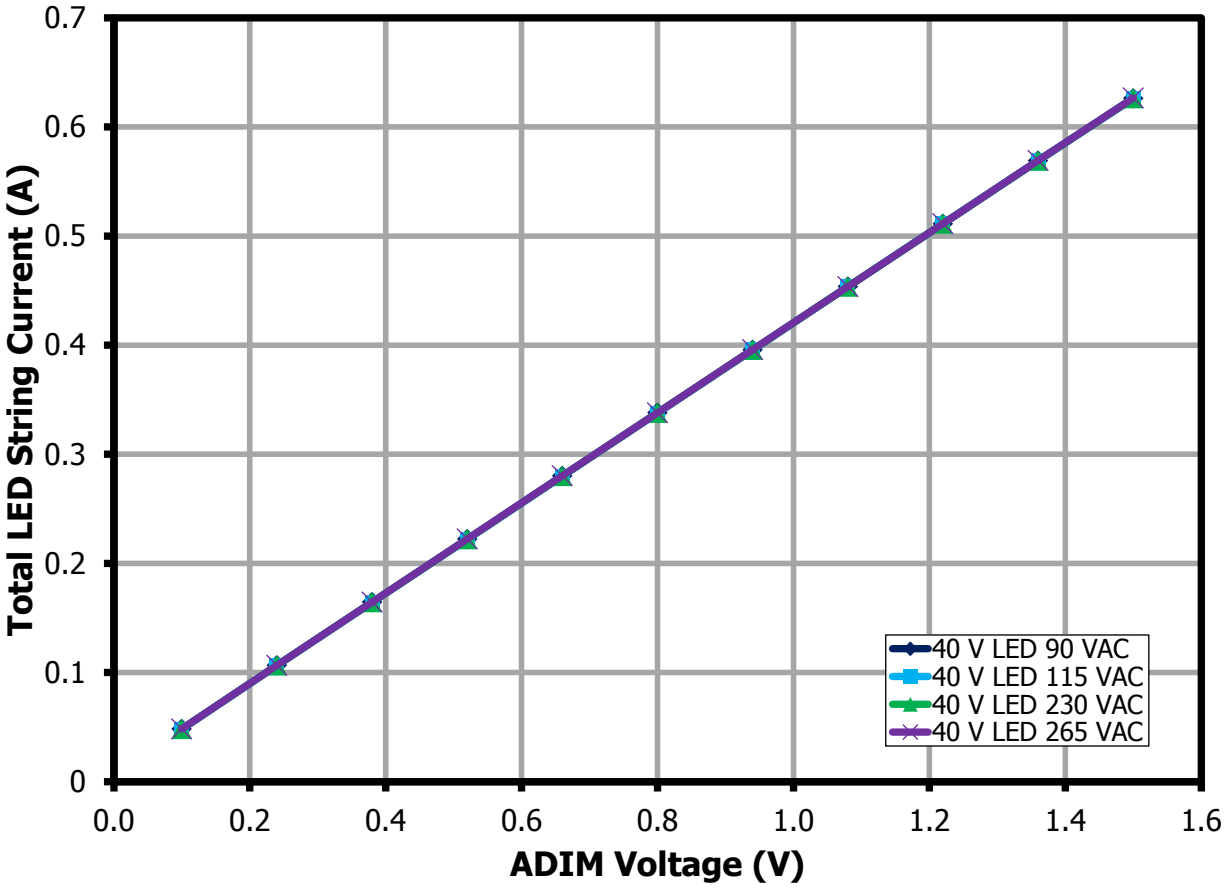

Figure 28 – Total LED Current vs. ADIM Input Voltage for 40 V LED Strings.

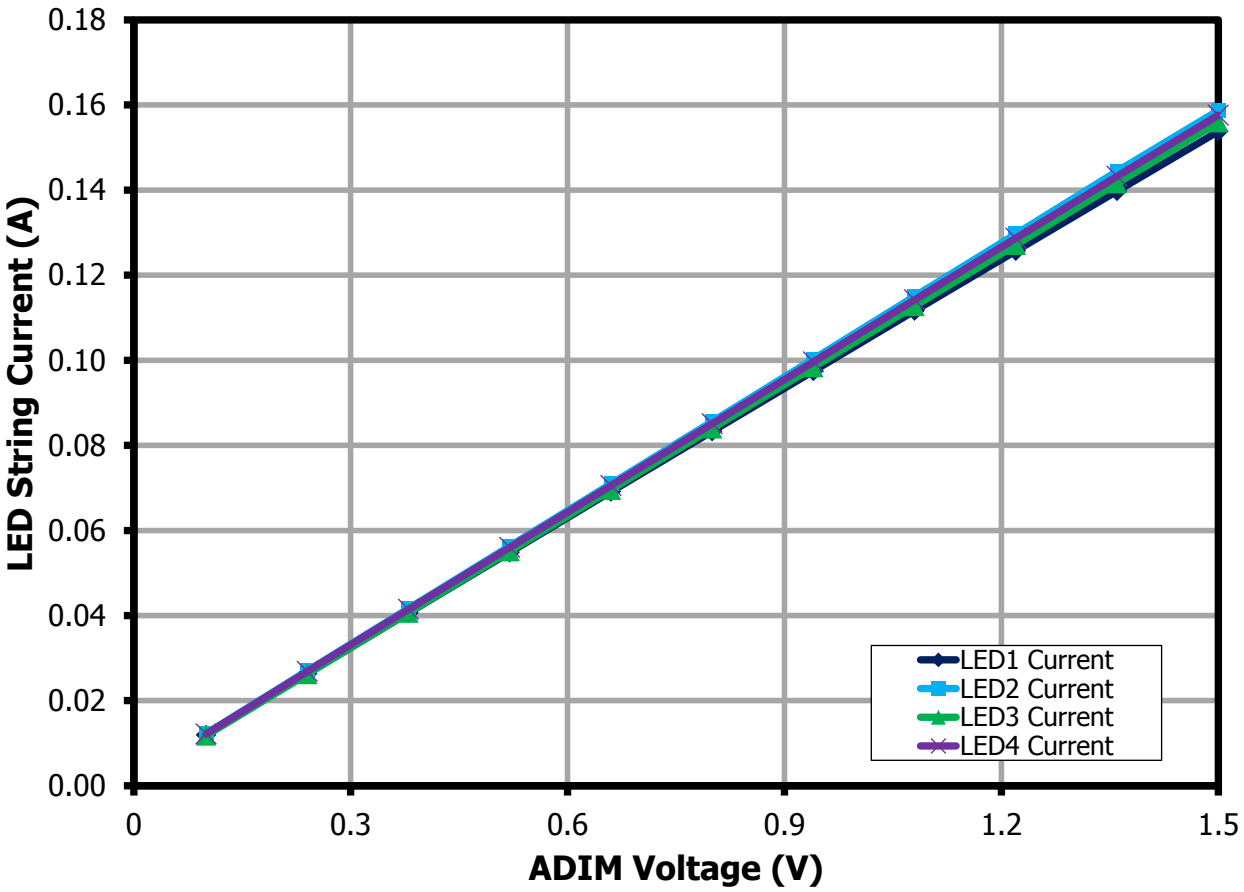

Figure 29 – 4 x 40 V String LED Current vs. ADIM Voltage at 90 VAC.

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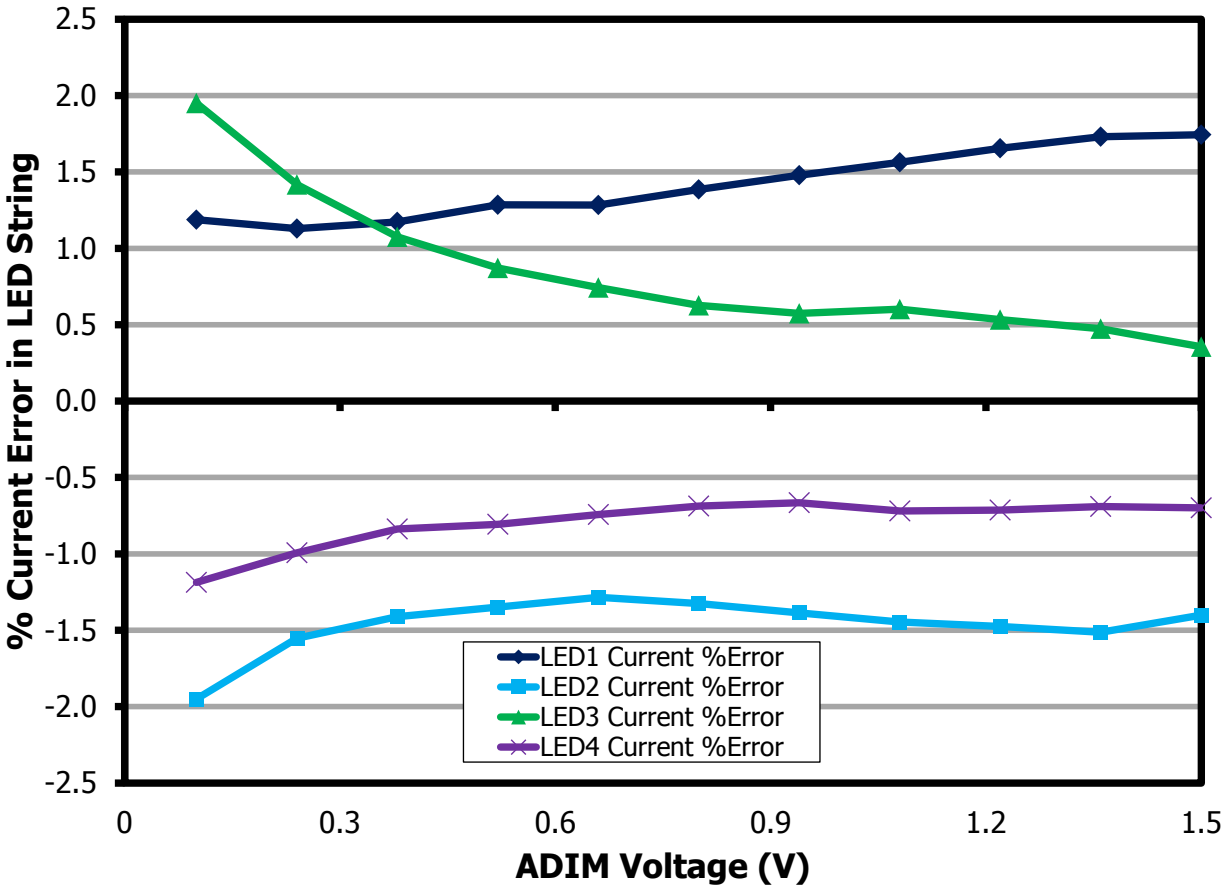

Figure 30 – LED String Current Matching Error for 40 V LED Strings at 90 VAC.

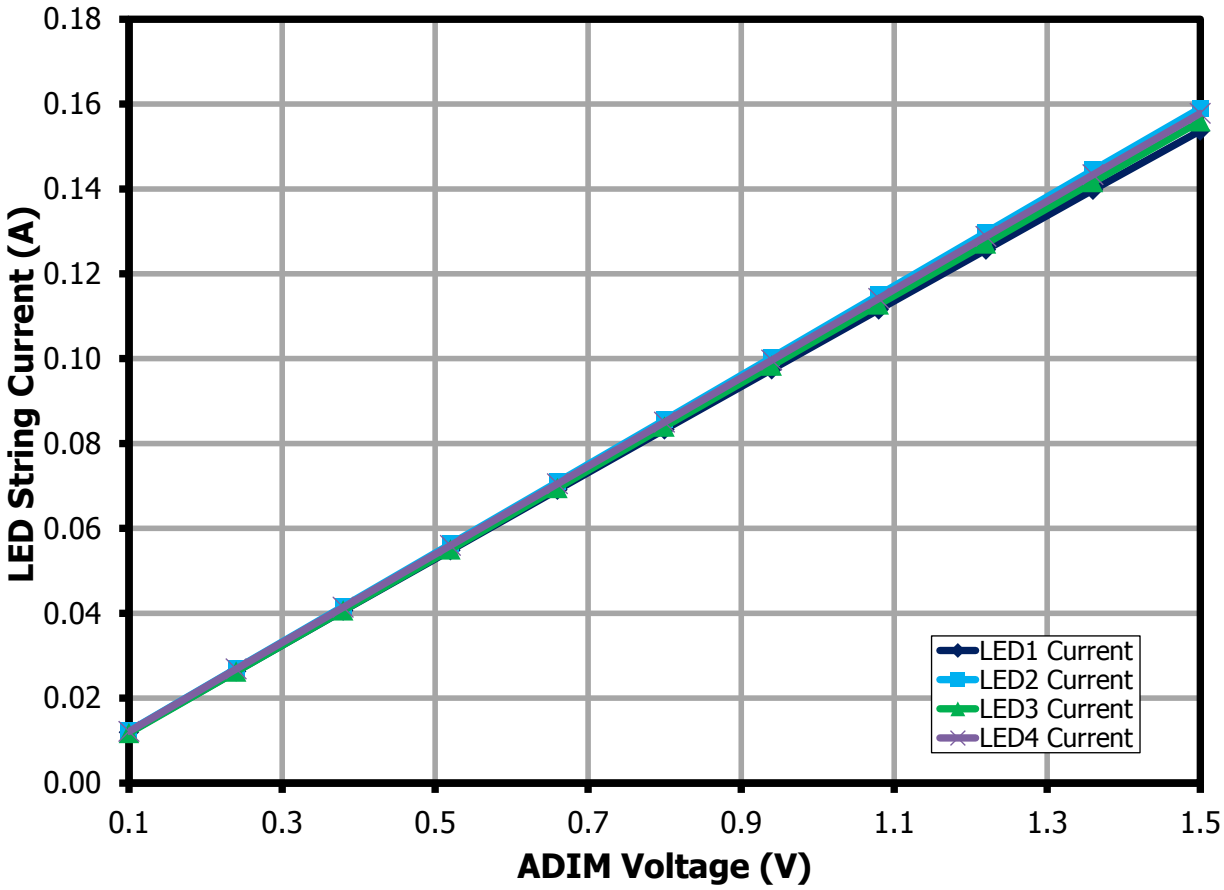

Figure 31 – 4 x 40 V String LED Current vs. ADIM Voltage at 115 VAC.

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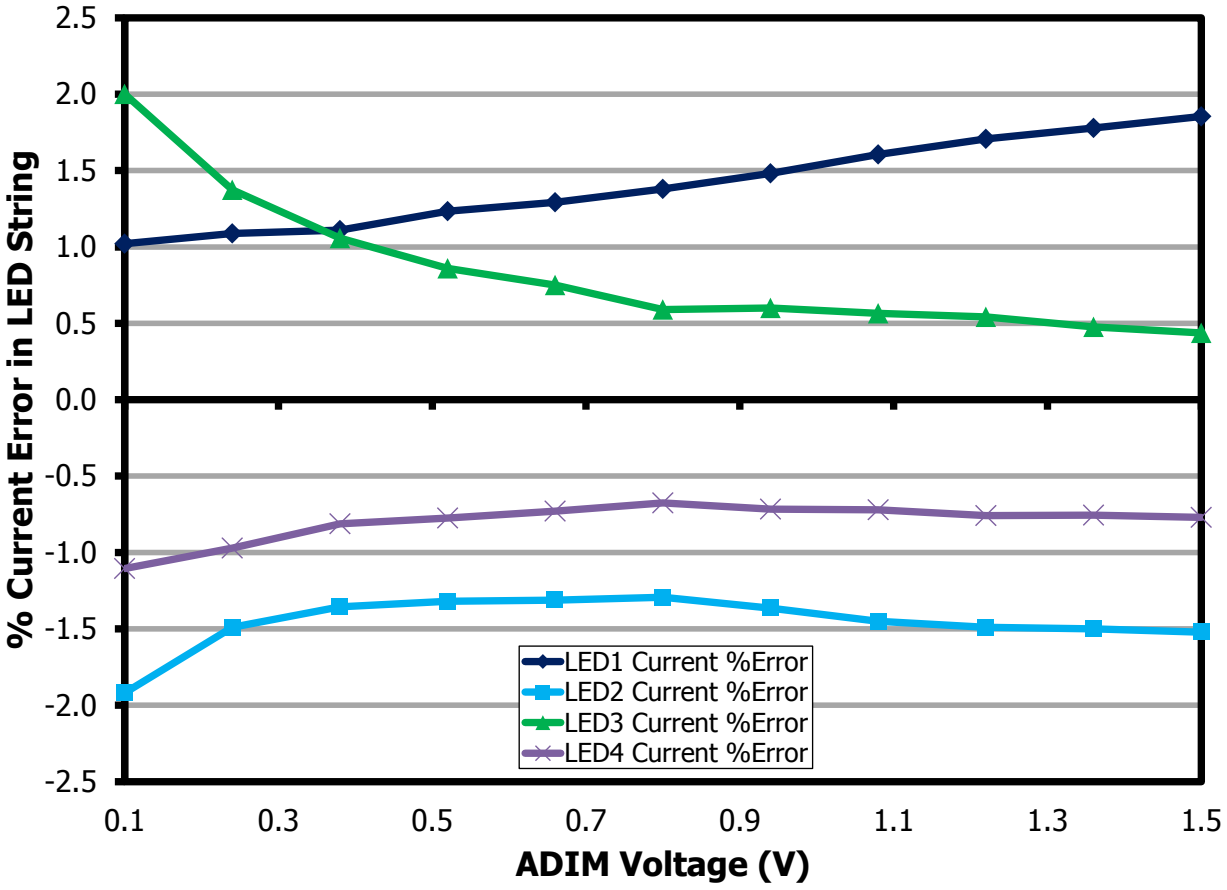

Figure 32 – LED String Current Matching Error for 40 V LED Strings at 115 VAC.

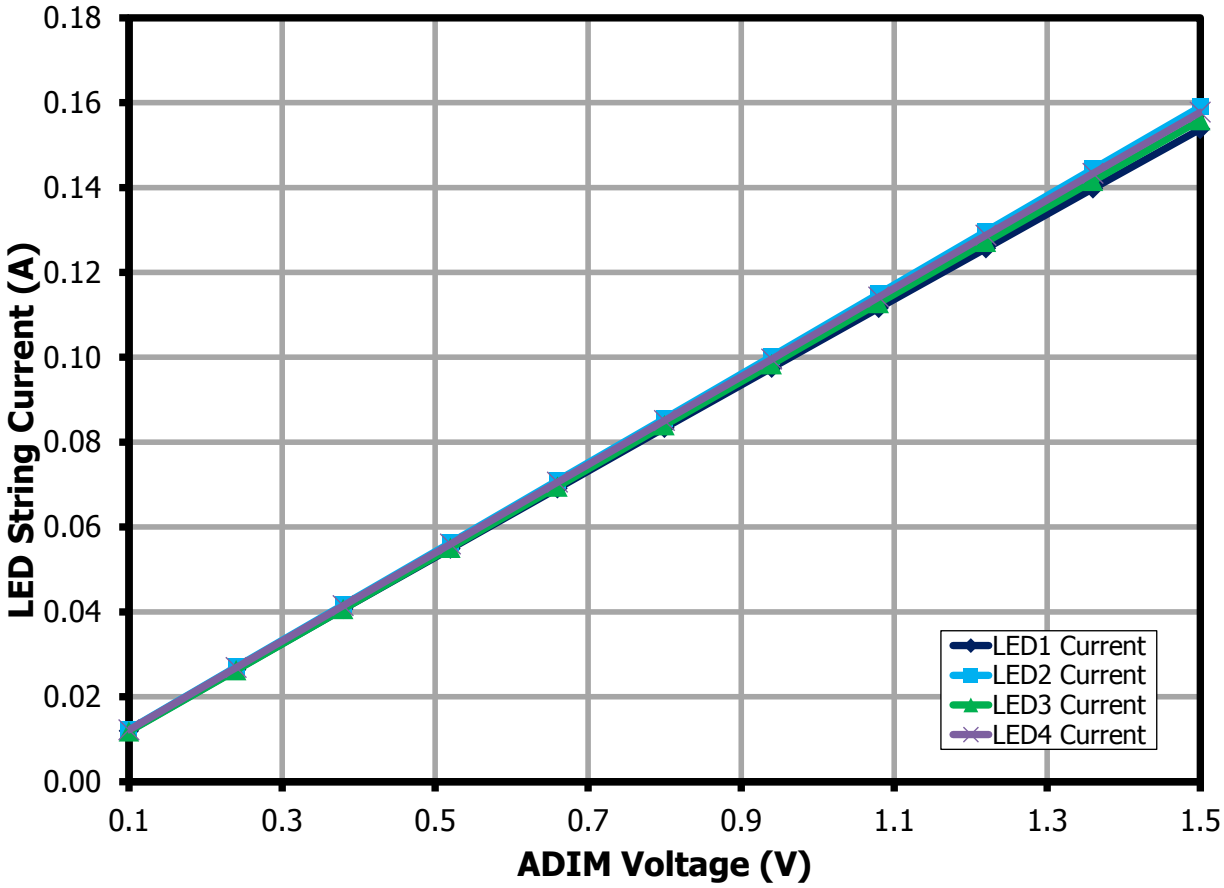

Figure 33 – 4 x 40 V String LED Current vs. ADIM Voltage at 230 VAC.

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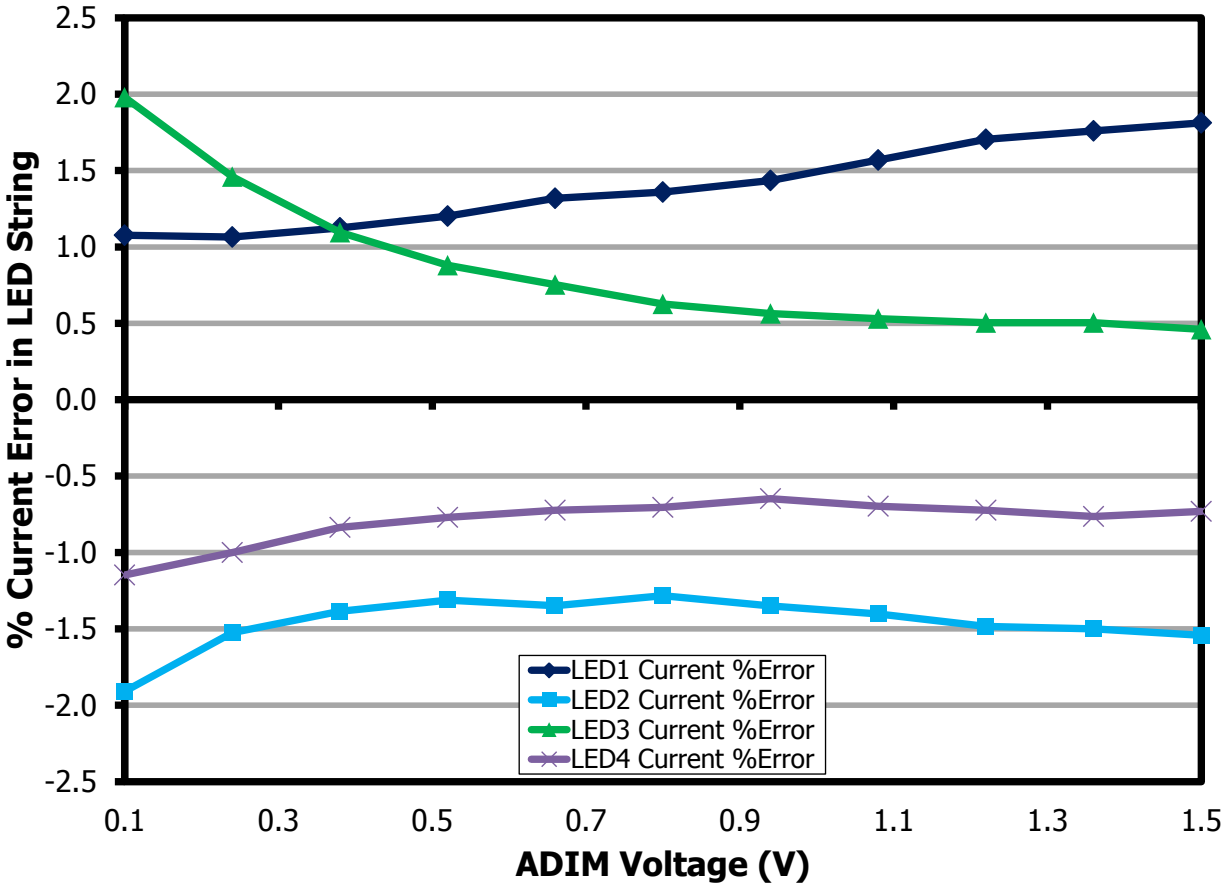

Figure 34 – LED String Current Matching Error for 40 V LED Strings at 230 VAC.

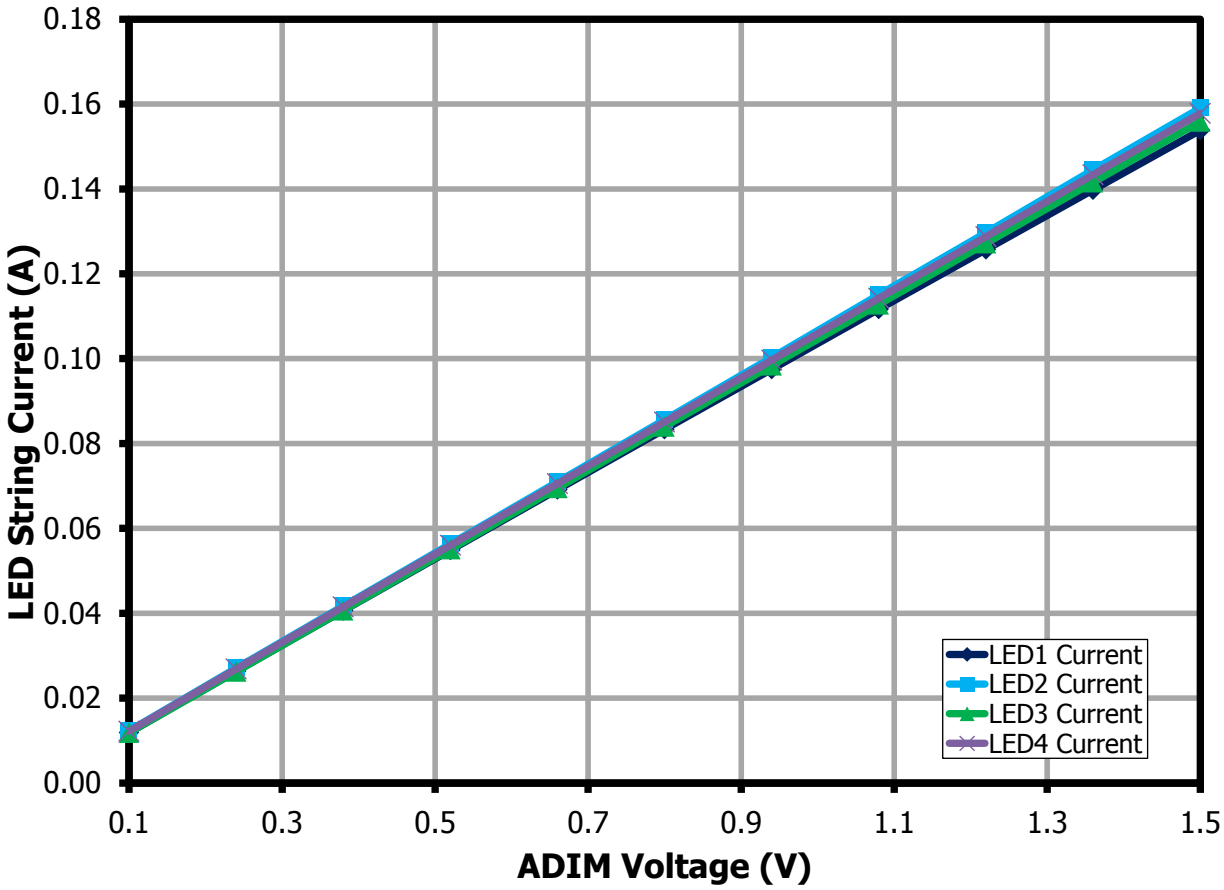

Figure 35 – 4 x 40 V String LED Current vs. ADIM Voltage at 265 VAC.

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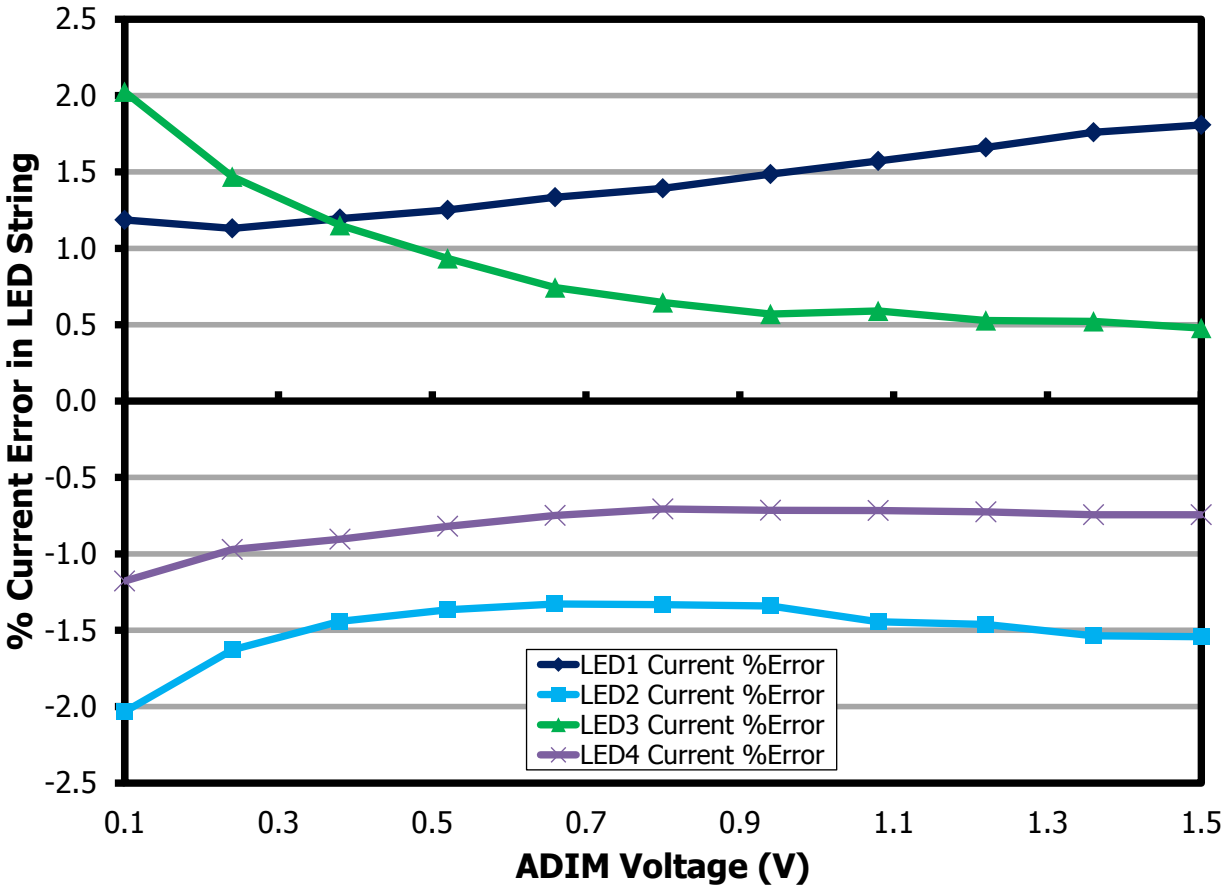

Figure 36 – LED String Current Matching Error for 40 V LED Strings at 265 VAC.

11.5 Input Power in Standby Mode and with 10 mA Load on 5 V

	VAC [V]				
I-VCV2 [mA]	**90**	6.5			
VCV2 [V]		6.43			
Pin [mW]		205			
f STDBY [kHz]		2.27			
V C30 [V]		8.5	*Primary bias voltage*		
V C31 [V]		5.41	*BPP pin*		
I-VCV2 [mA]	**115**	6.5			
VCV2 [V]		6.38			
Pin [mW]		209			
f STDBY [kHz]		2.4			
V C30 [V]		8.49	*Primary bias voltage*		
V C31 [V]		5.42	*BPP pin*		
I-VCV2 [mA]	**230**	6			
VCV2 [V]		6.2			
Pin [mW]		244			
f STDBY [kHz]		1.69			
V C30 [V]		8.57	*Primary bias voltage*		
V C31 [V]		5.43	*BPP pin*		
I-VCV2 [mA]	**265**	6			
VCV2 [V]		6.15	*10.49V at full load*		
Pin [mW]		262			
f STDBY [kHz]		1.35			
V C30 [V]		8.58	*Primary bias voltage*		
V C31 [V]		5.43	*BPP pin*		

Table 9 - Standby Mode Test Results

Input power, primary and secondary bias voltage, secondary bias current and switching frequency in Standby Mode.

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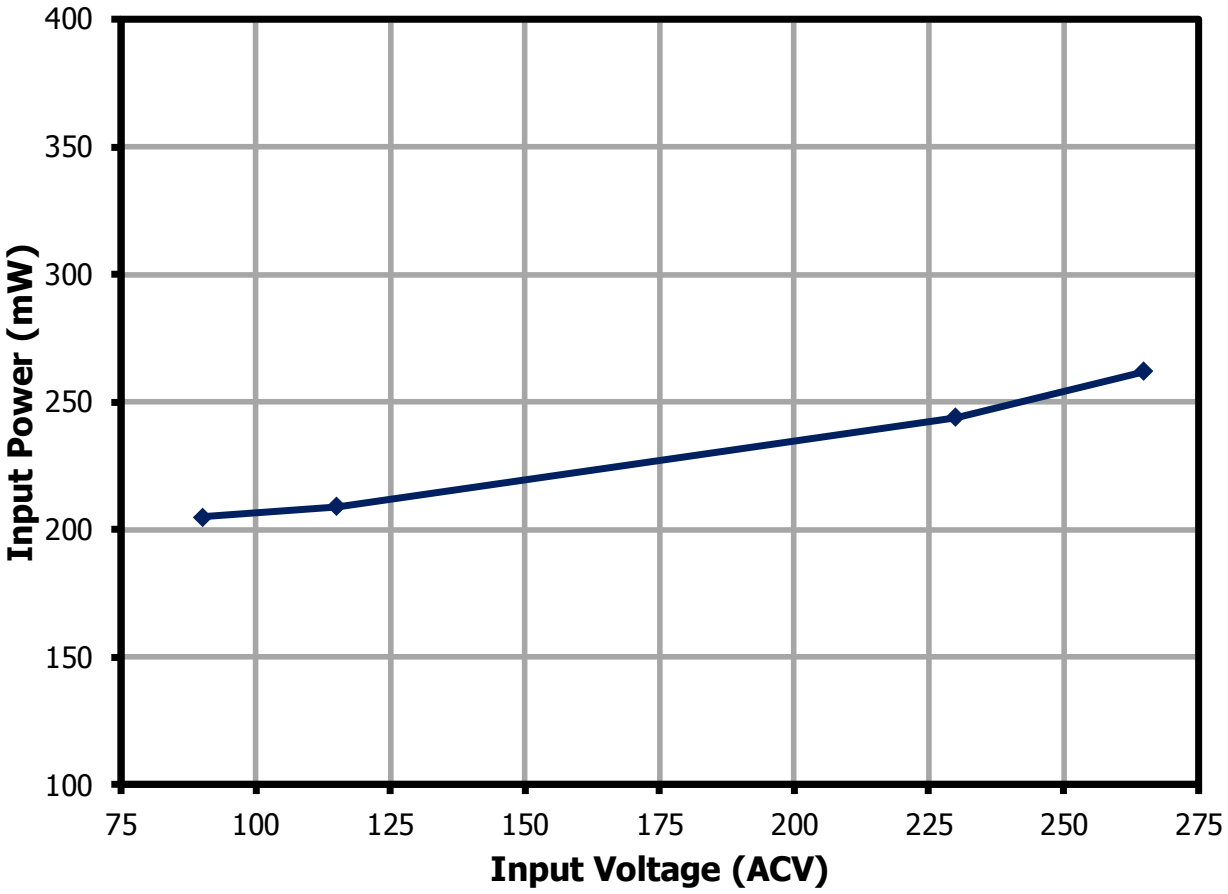

Figure 37 – Input Power vs. Input Voltage, Room Temperature.

12 Waveforms

12.1 Load Transient Response

Test was performed at 230 VAC, CV1 load set to 3 A, 40 V LED panel used.

50 mA – 3 A – 50 mA transient load applied to CV1 output at a 10 Hz rate, 50% duty cycle.

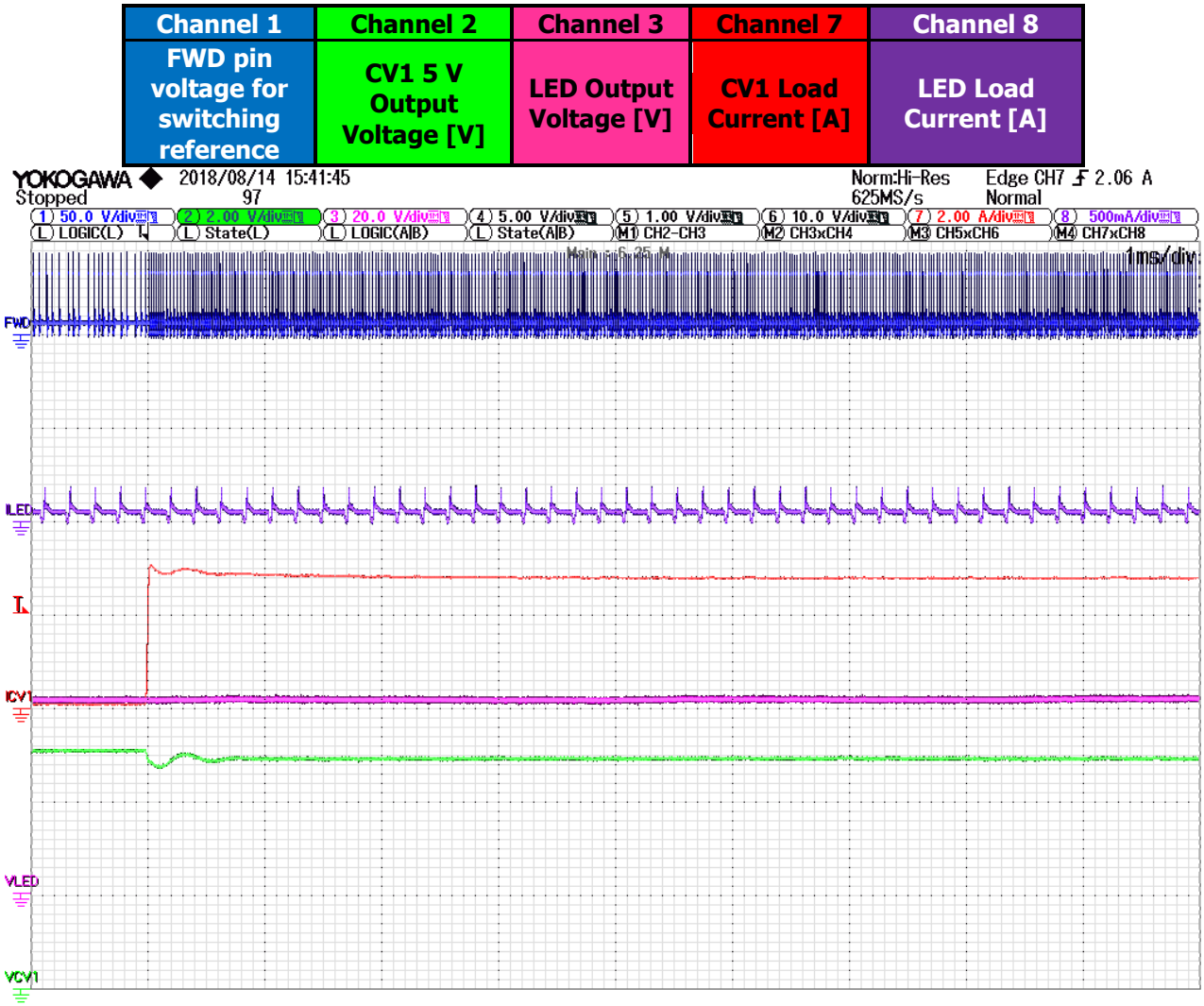

Figure 38 –5 V Output Load Transient 50 mA to 3 A with 63 mA Total LED Current.

Supply voltage=230 VAC.

Resulting undershoot=315 mV.

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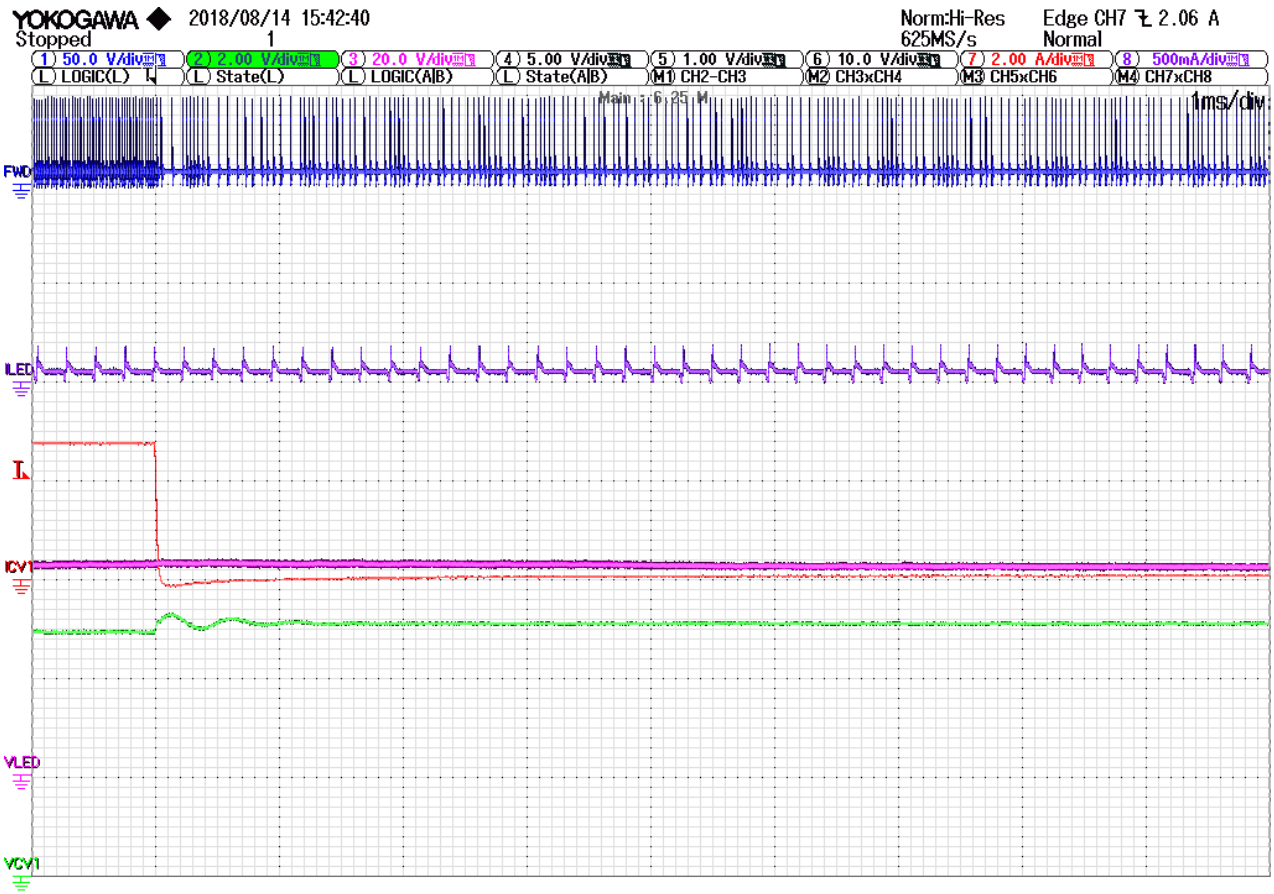

Figure 39 – 5 V Output Load Transient 3A to 50 mA with 63 mA Total LED Current.

Supply voltage=230 VAC.

Resulting undershoot=330 mV.

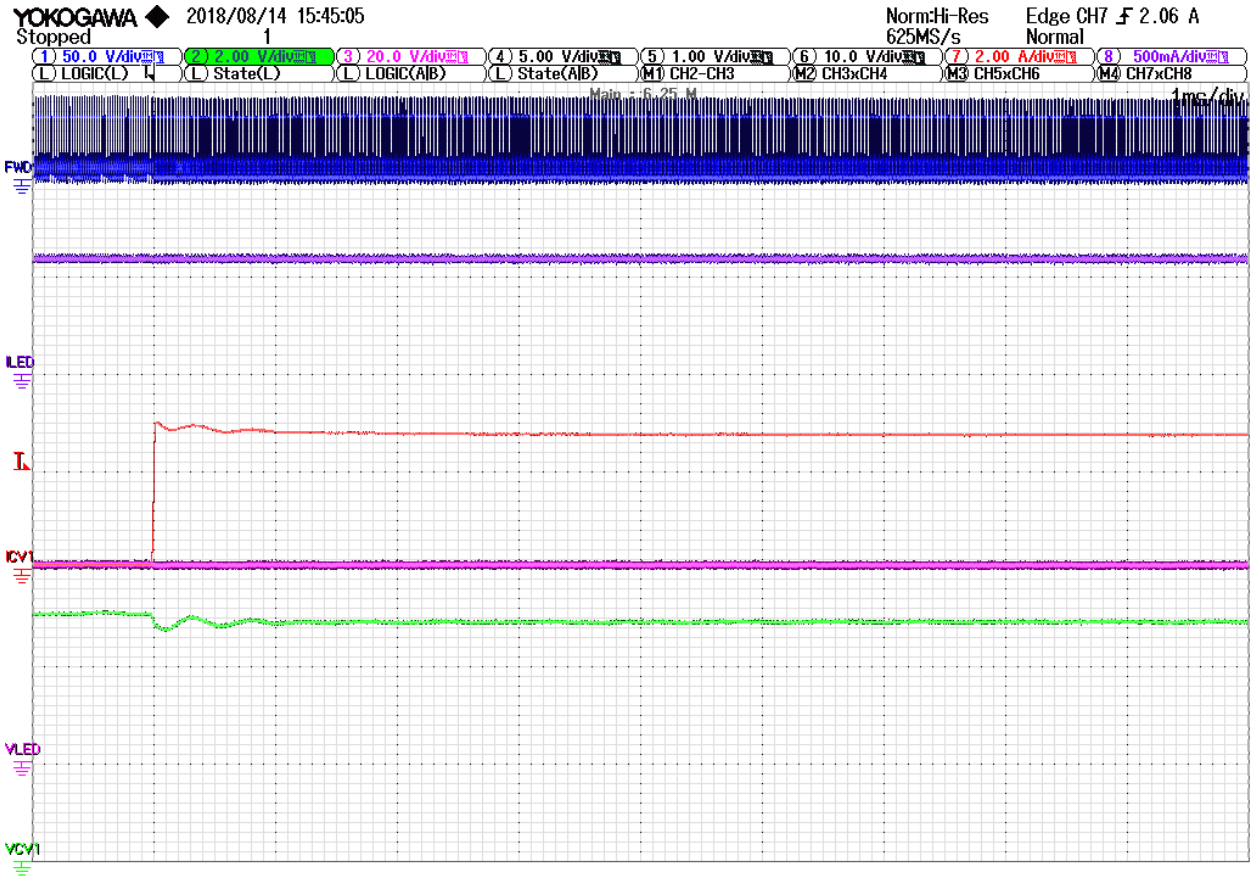

Figure 40 – 5 V Output Load Transient 50 mA to 3 A with 625 mA Total LED Current.

Supply voltage=230 VAC.

Resulting undershoot=235 mV.

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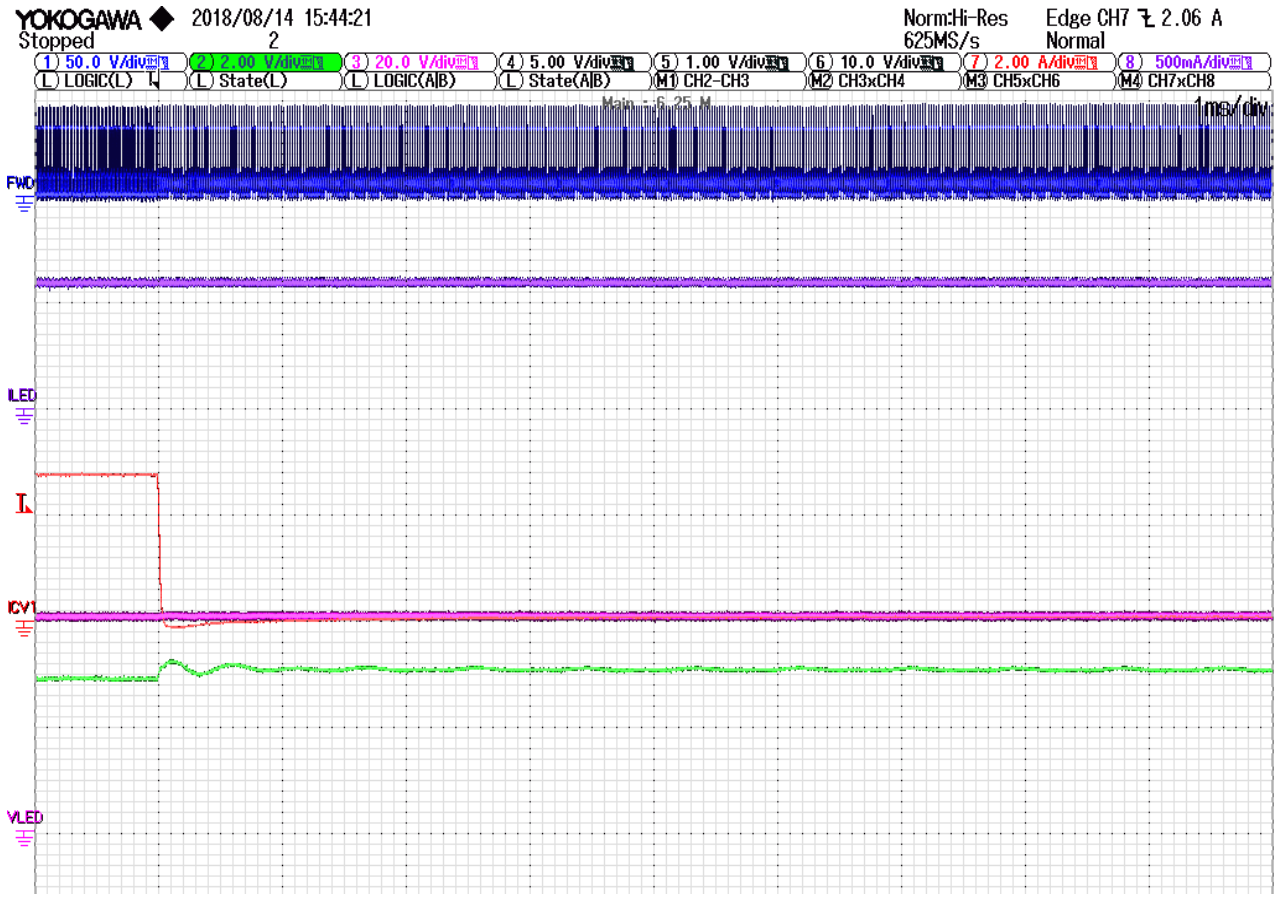

Figure 41 – 5 V Output Load Transient 3A to 50 mA with 625 mA Total LED Current.

Supply voltage=230 VAC.

Resulting overshoot=215 mV.

12.2 Switching Waveforms

12.2.1 InnoSwitch3-MX Voltage Waveforms

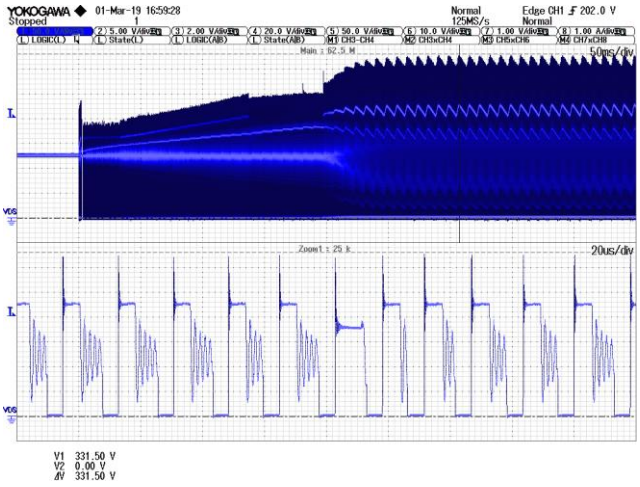

Figure 42 – Drain Voltage Waveforms.
90 VAC Input, Full Load, (331 V_{MAX}).

V_{DRAIN}, 50 V, 50 ms, 20 μs / div.

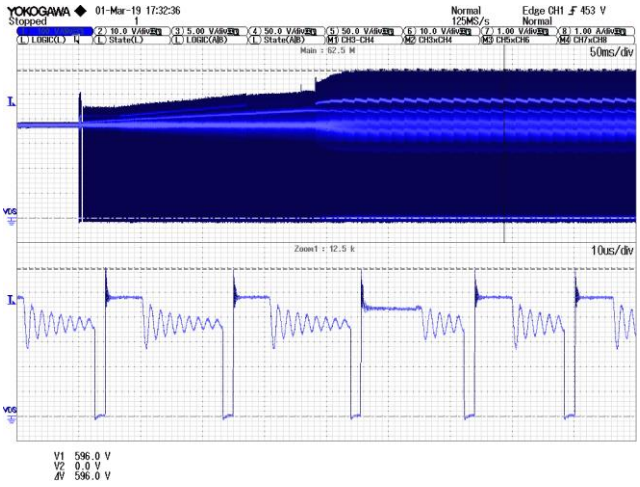

Figure 43 – Drain Voltage Waveforms.
265 VAC Input, Full Load, (596 V_{MAX}).

Upper: V_{DRAIN}, 100 V, 50 ms, 10 μs / div.

12.2.2 SR FET Voltage Waveforms

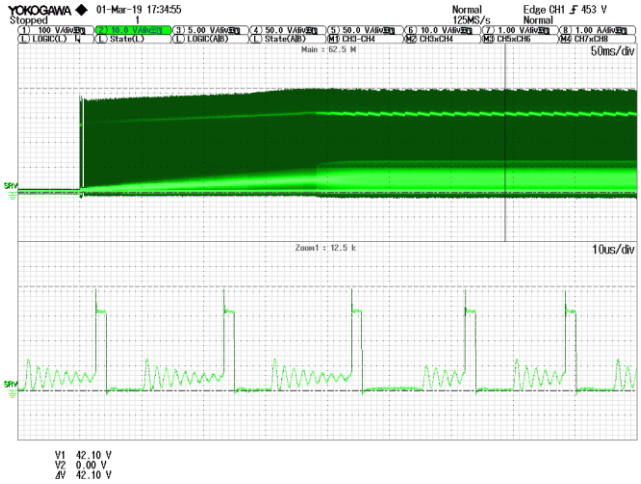

Figure 44 – SR FET Voltage Waveforms.
265 VAC Input, Full Load, (42.1 V_{MAX}).

V_{DS}: 10 V / 50 ms, 10 μs / div.

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12.2.3 Q1 5 V Selection MOSFET Voltage Waveforms

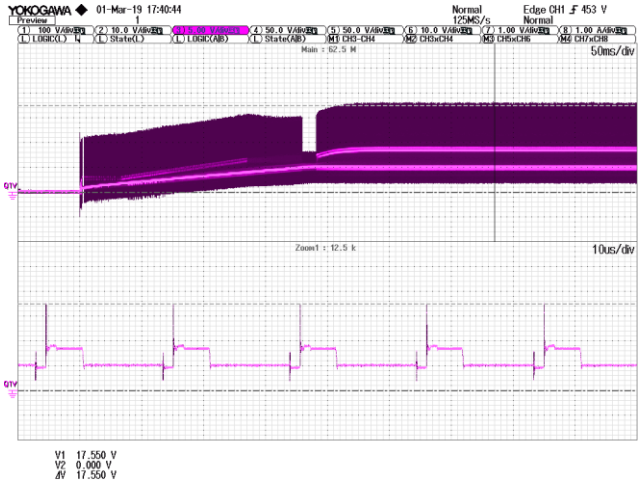

Figure 45 – Q1 Selection MOSFET Voltage Waveforms, 265 VAC Input.

Full Load (12.55 V_{MAX}), (-4.8V –ve max).
V_{DS}: 5 V / 50 ms, 10 μs / div.

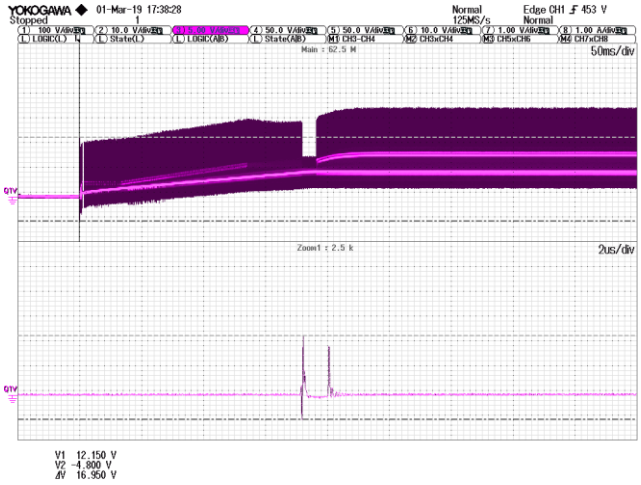

Figure 46 – Q1 Selection MOSFET Voltage Waveforms During Start-Up.

2nd Pulse is Worst Case.
265 VAC Input, Full Load (25 V_{MAX}).
V_{DS} : 5 V / 50 ms, 2 μs / div.

12.2.4 D3, LED Output Diode Voltage Waveforms

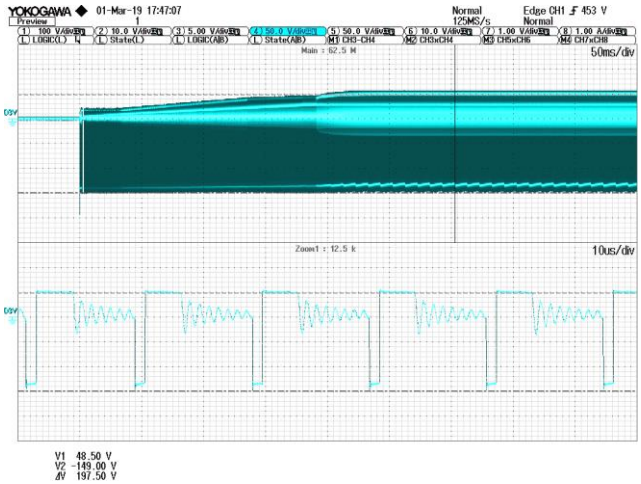

Figure 47 – D3, LED Output Diode Voltage Waveforms, 265 VAC Input.

Full Load (197.5 V_{MAX}),
V_{DS}: 50 V / 50 ms, 10 μs / div.

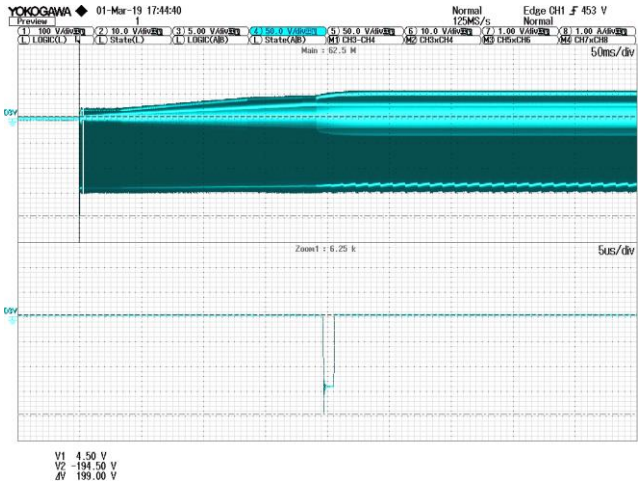

Figure 48 – D3, LED Output Diode Voltage Waveforms During Start-Up.

2nd Pulse is Worst Case.
265 VAC Input, Full Load (199 V_{MAX}).
V_{DS}: 50 V / 50 ms, 5 μs / div.

12.2.5 Start-Up Waveforms

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 8
Pri FET Vds [V]	CV1 5V Output [V]	V led Output [V]	BP5V [V]	U1/2 REQ pin [V]	U1/2 ACK pin [V]	LED Output Current [A]

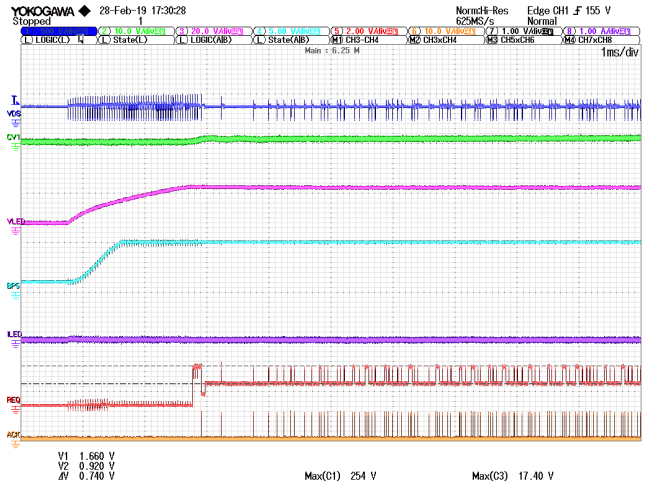

Figure 49 – Input 90 VAC. Initial Start-up 1st 10 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

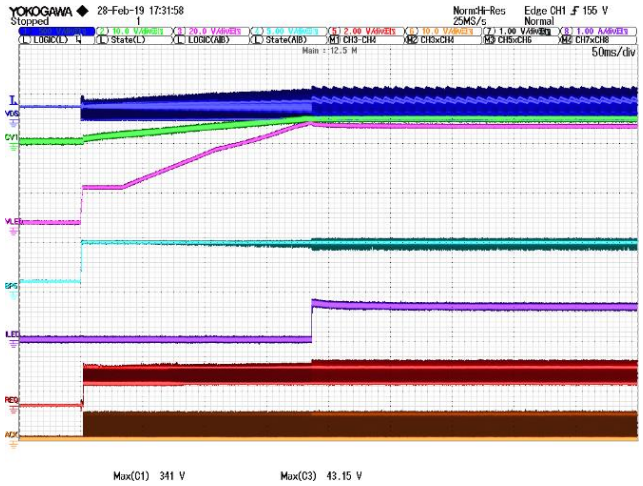

Figure 50 – Input 90 VAC. Full Start-Up Over 500 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

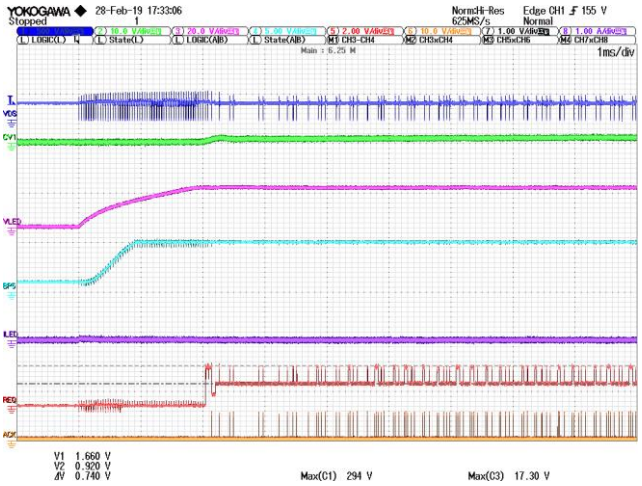

Figure 51 – Input 115 VAC. Initial Start-up 1st 10 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

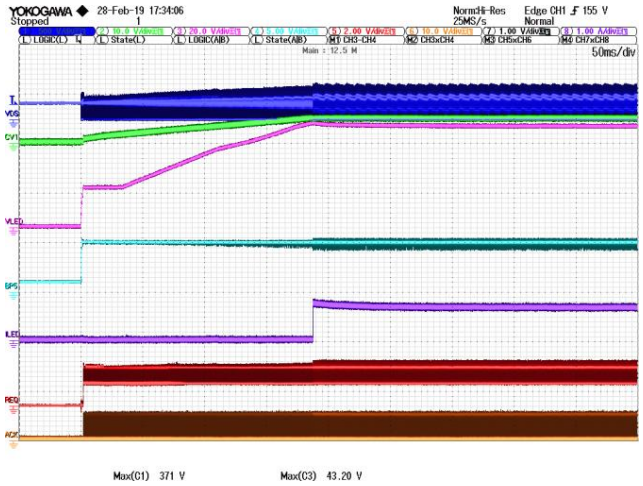

Figure 52 – Input 115 VAC. Full Start-Up Over 500 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

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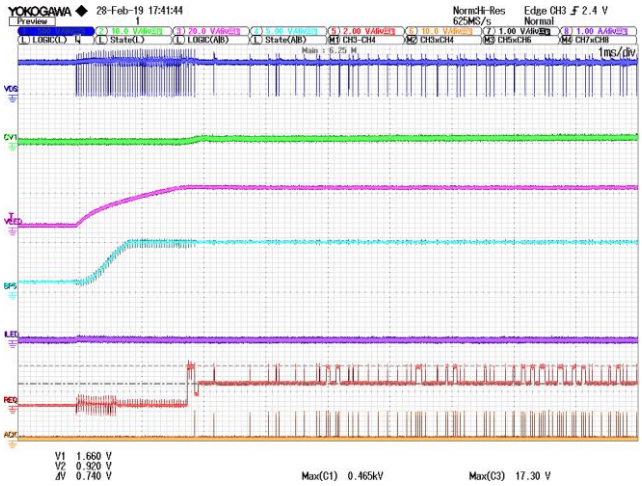

Figure 53 – Input 230 VAC. Initial Start-up 1st 10 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

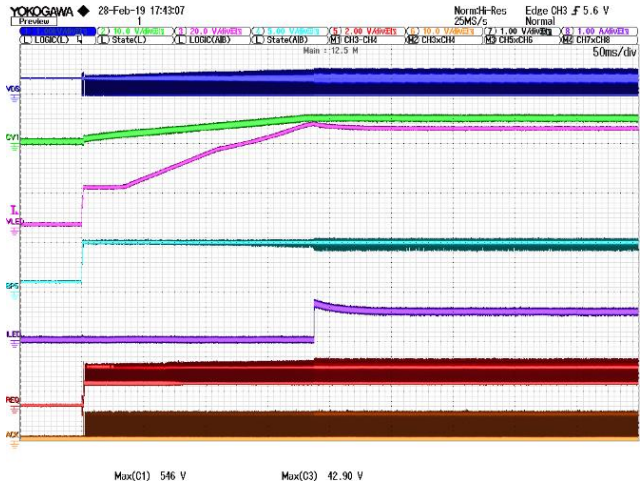

Figure 54 – Input 230 VAC. Full Start-Up over 500 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

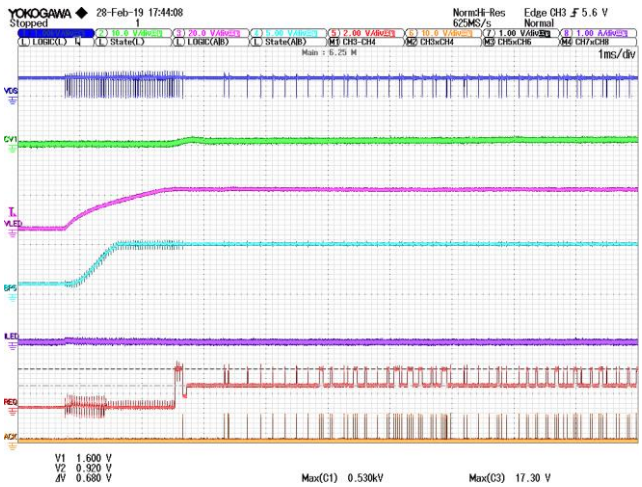

Figure 55 – Input 265 VAC. Initial Start-up 1st 10 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

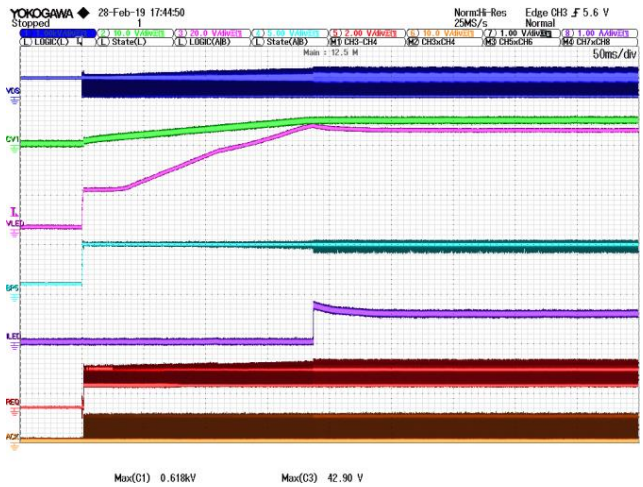

Figure 56 – Input 265 VAC. Full Start-Up over 500 ms.

Output CV1 = 5 V @ 15 W,
LED = 40 V @ 625 mA.

12.2.6 Start-Up in Standby

Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 8
Pri FET Vds [V]	CV1 5V Output [V]	V led Output [V]	BP5V [V]	U1/2 REQ pin [V]	U1/2 ACK pin [V]	LED Output Current [A]

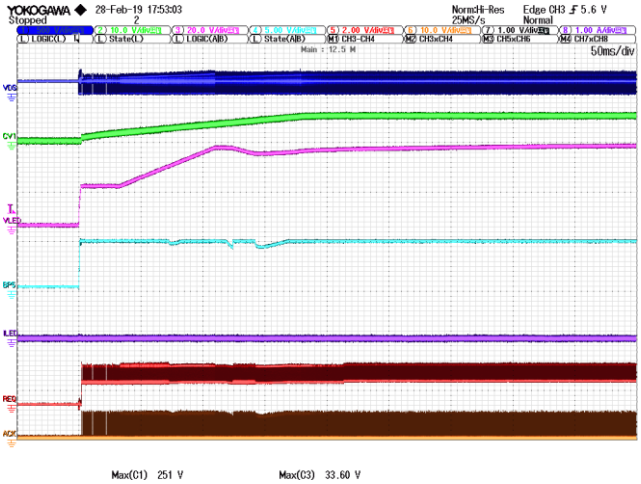

Figure 57 – Input 90 VAC. Full Start-Up over 500 ms.

Output CV1 = 5 V @ 15 mA,
LED = Standby.

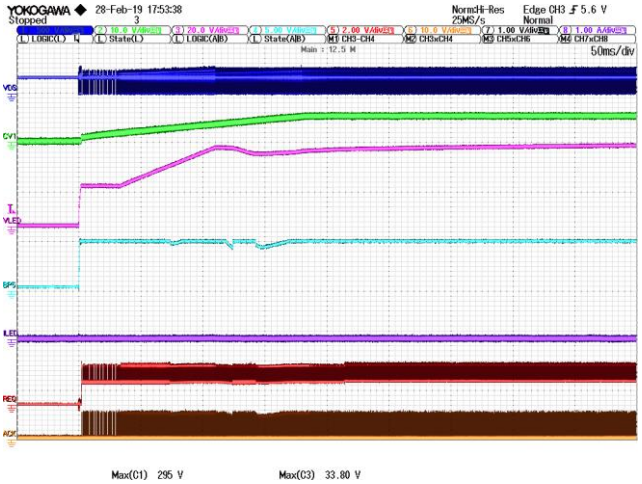

Figure 58 – Input 115 VAC. Full Start-Up over 500 ms.

Output CV1 = 5 V @ 15 mA,
LED = Standby.

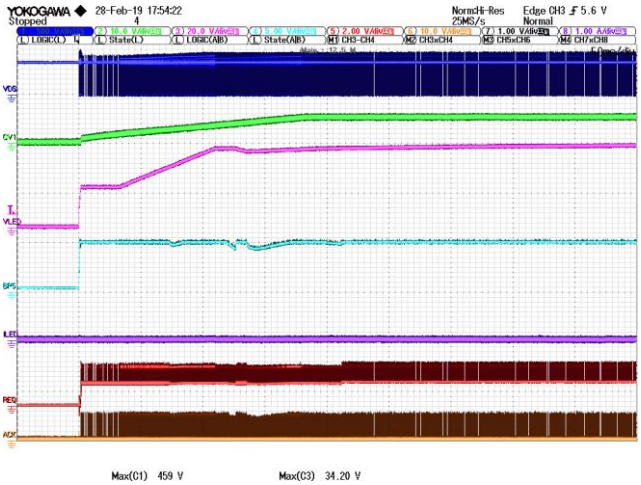

Figure 59 – Input 230 VAC. Full Start-Up over 500 ms.

Output CV1 = 5 V @ 15 mA,
LED = Standby.

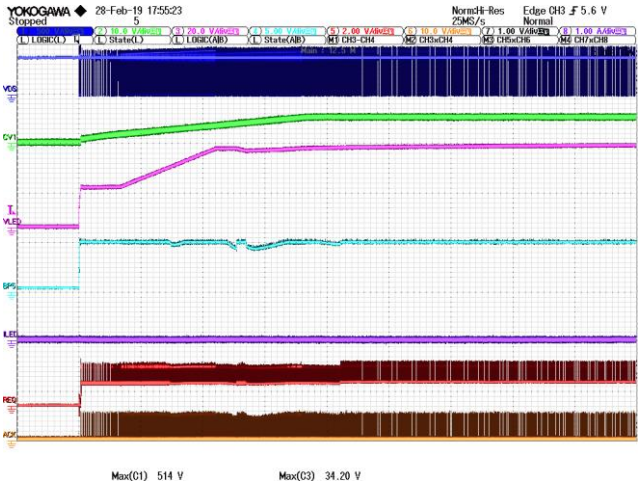

Figure 60 – Input 265 VAC. Full Start up over 500 ms.

Output CV1 = 5 V @ 15 mA,
LED = Standby.

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12.3 Brown-In and Brown-Out

Channel 1	Channel 2	Channel 3
AC Input Voltage	LED Output Voltage [V]	CV1 5 V Output Voltage [V]

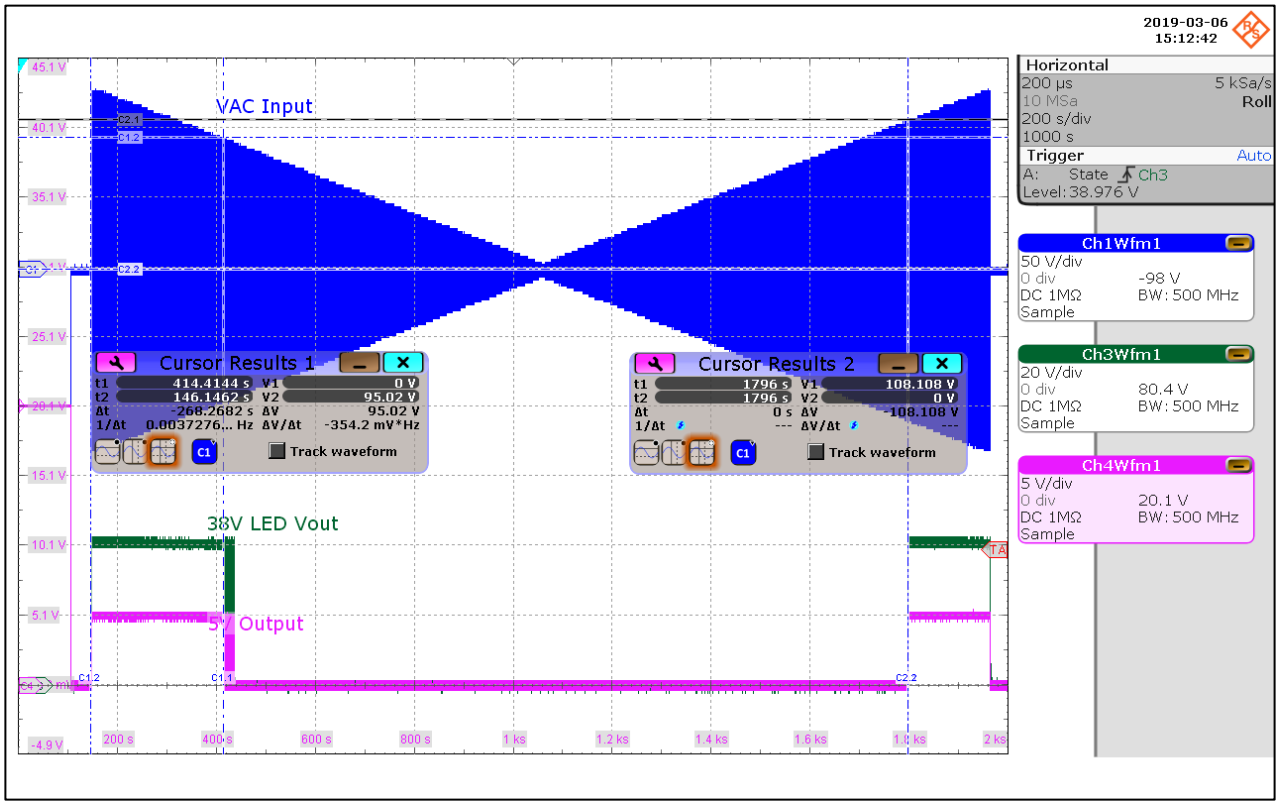

Figure 61 – Brown-In and Brown-Out response, 90 VAC – 0 VAC – 90 VAC.

VAC Input (VAC)	Brown In Peak Voltage (V_{PK})	Brown In RMS Voltage (V_{RMS})	Brown Out Peak Voltage (V_{PK})	Brown Out RMS Voltage (V_{RMS})
90	106.96	75.63	94.00	66.47

Table 10 - Brown-In and Brown-Out response, 90 VAC – 0 VAC – 90 VAC Results

Channel 1	Channel 2	Channel 3
AC Input Voltage	LED Output Voltage [V]	CV1 5 V Output Voltage [V]

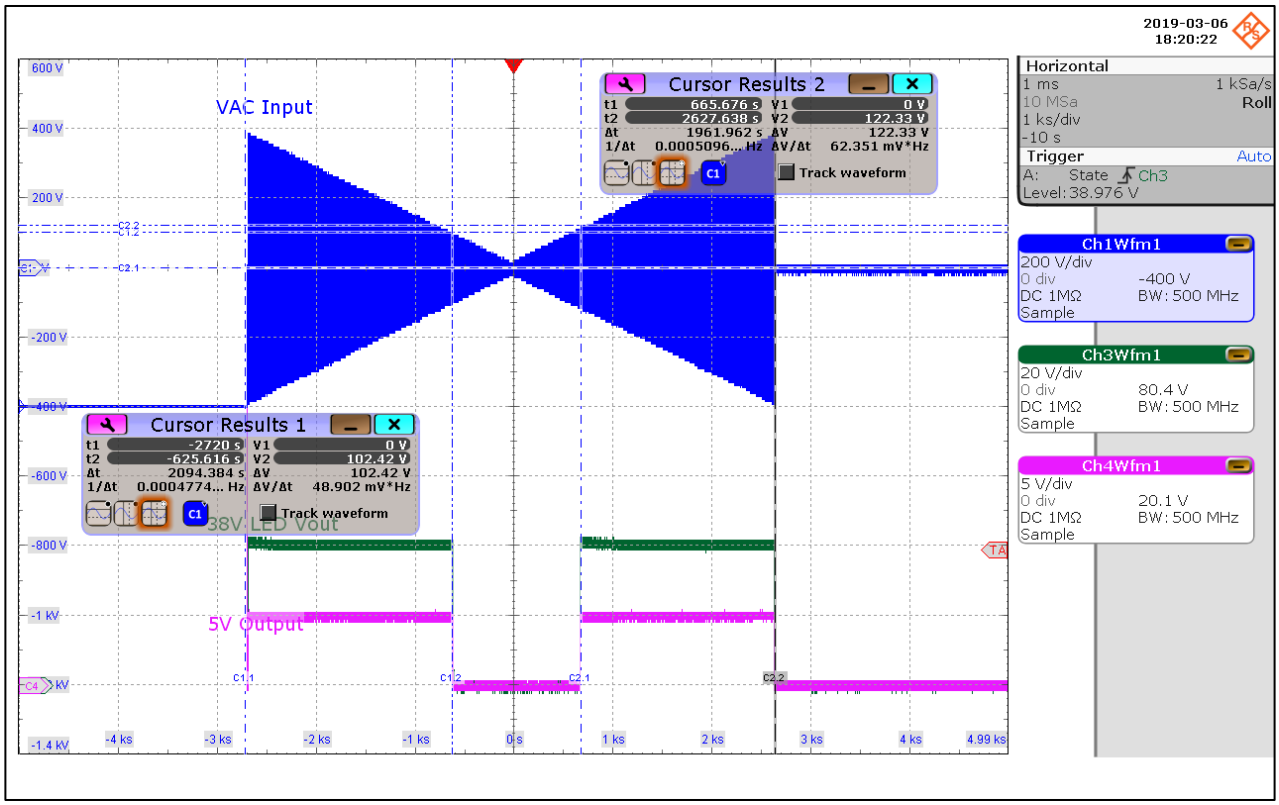

Figure 62 – Brown-In and Brown-Out response, 265 VAC – 0 VAC – 265 VAC.

VAC Input (VAC)	Brown In Peak Voltage (V_{PK})	Brown In RMS Voltage (V_{RMS})	Brown Out Peak Voltage (V_{PK})	Brown Out RMS Voltage (V_{RMS})
265	106.27	75.15	94.04	66.50

Table 11 – Brown-In and Brown-Out response, 265 VAC – 0 VAC – 265 VAC Results.

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12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was used in order to reject noise pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/100 V ceramic type and one (1) 10 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

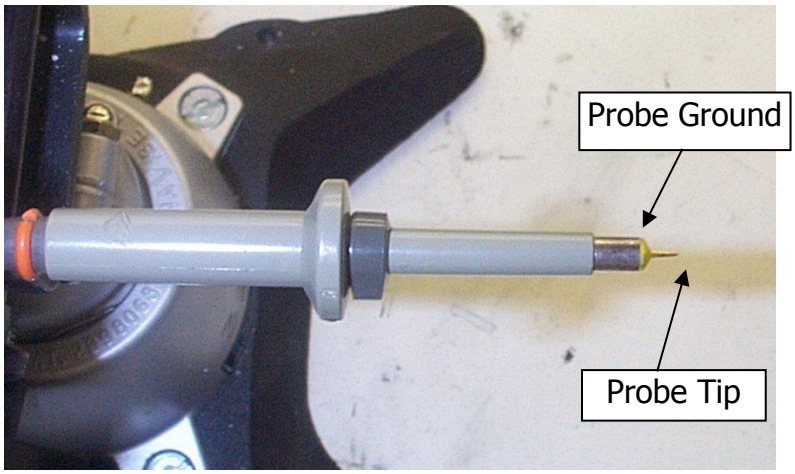

Figure 63 – Oscilloscope Probe Prepared for Ripple Measurement.

(End Cap and Ground Lead Removed)

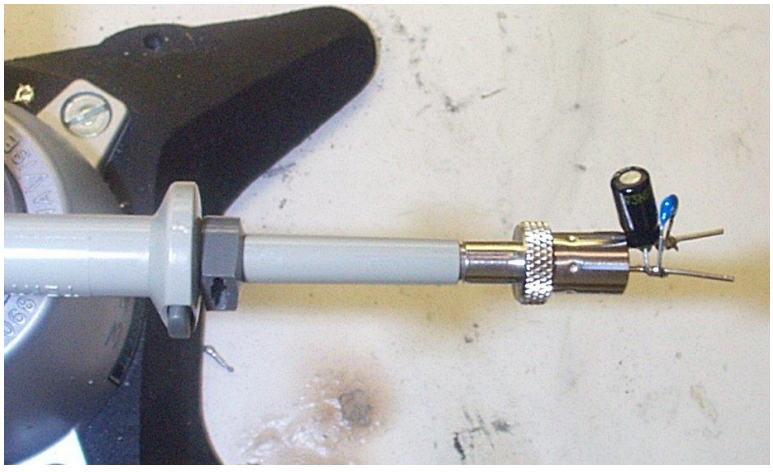

Figure 64 – Oscillocope Probe with modified BNC Adapter.

Probe Master **(**www.probemaster.com**)** 4987A BNC Adapter.

(Modified by adding two parallel decoupling capacitors and wires for ripple measurement)

12.4.1.1 Output CV1 (5 V) Voltage Ripple and noise.

12.4.1.1.1 CV1 = 5 V 3 A, LED = 40 V 625 mA

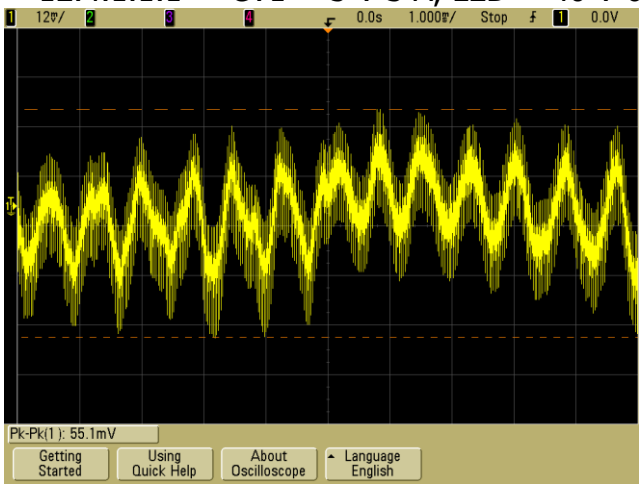

Figure 65 – V_{IN} = 90 VAC. V_{RIPPLE_CV1} = 55.1 mV_{PK-PK}.
CH1: V_CV1, 12 mV / div. (ac) , 1 ms / div.

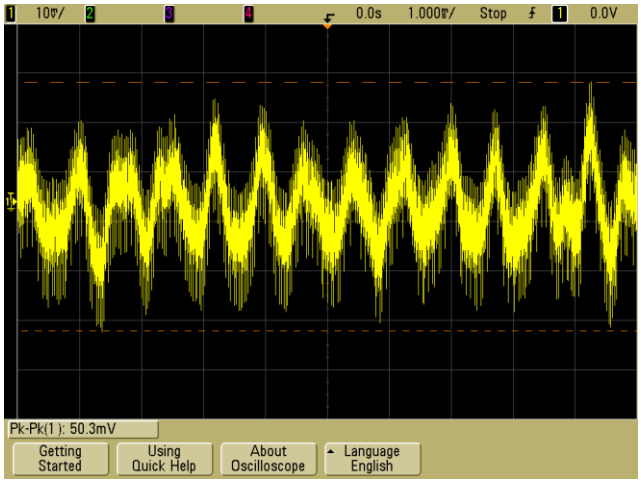

Figure 66 – V_{IN} = 115 VAC. V_{RIPPLE_CV1} = 50.3 mV_{PK-PK}.
CH1: V_CV1, 10 mV / div. (ac) , 1 ms / div.

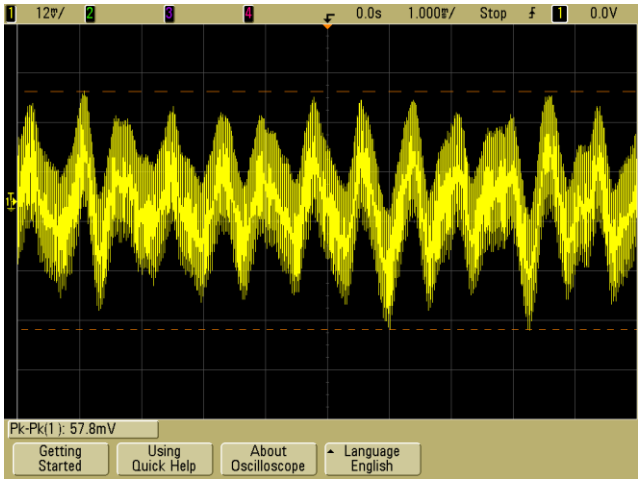

Figure 67 – V_{IN} = 230 VAC. V_{RIPPLE_CV1} = 57.8 mV_{PK-PK}.
CH1: V_CV1, 12 mV / div. (ac) , 1 ms / div.

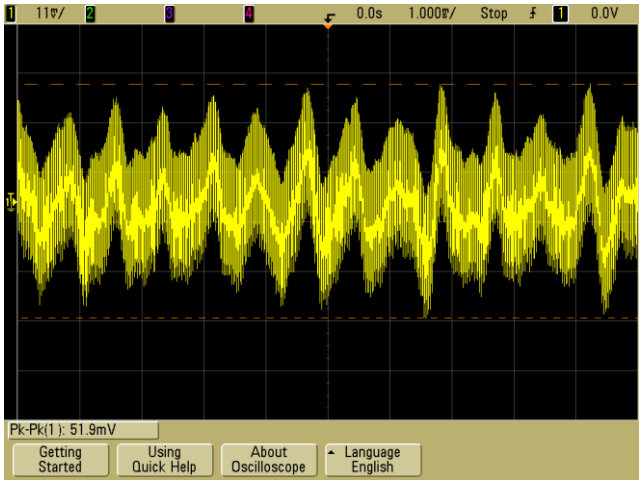

Figure 68 – V_{IN} = 265 VAC. V_{RIPPLE_CV1} = 51.9 mV_{PK-PK}.
CH1: V_CV1, 10 mV / div. (ac) , 1 ms / div.

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12.4.1.1.2 CV1 = 5 V 3 A, LED = 3 0 V 625 mA

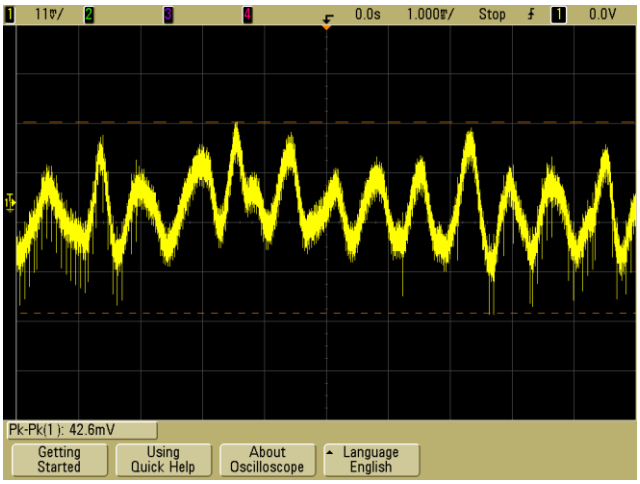

Figure – V_{IN} = 90 VAC. V_{RIPPLE_CV1} = 42.6 mV_{PK-PK}. CH1: V_CV1, 11 mV / div. (ac) , 1 ms / div.

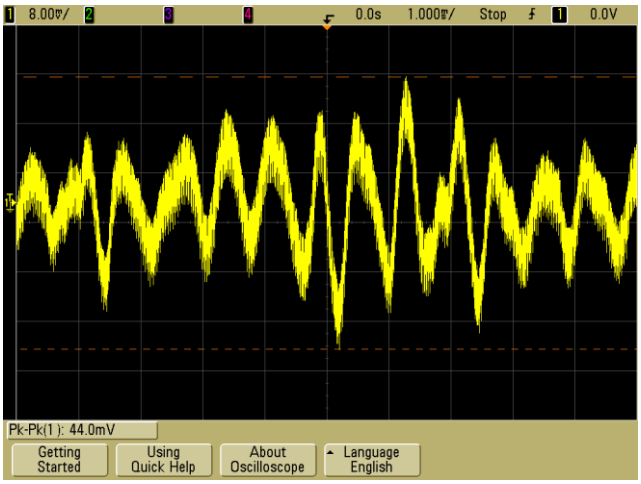

Figure 69 – V_{IN} = 115 VAC. V_{RIPPLE_CV1} = 44.0 mV_{PK-PK}. CH1: V_CV1, 8 mV / div. (ac) , 1 ms / div.

Figure 70 – V_{IN} = 230 VAC. V_{RIPPLE_CV1} = 49.1 mV_{PK-PK}. CH1: V_CV1, 10 mV / div. (ac) , 1 ms / div.

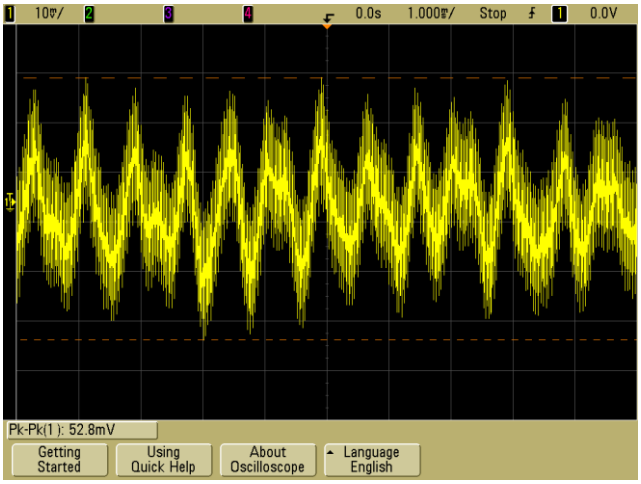

Figure 71 – V_{IN} = 265 VAC. V_{RIPPLE_CV1} = 52.8 mV_{PK-PK}. CH1: V_CV1,10 mV / div. (ac) , 1 ms / div.

13 Conducted Emissions with Output GND Connected to Ground Plane.

Blue trace – Quasi Peak Detector, highest measurement on L1 or N AC input.
Green trace – Average Detector, highest measurement on L1 or N AC input.

13.1 115VAC

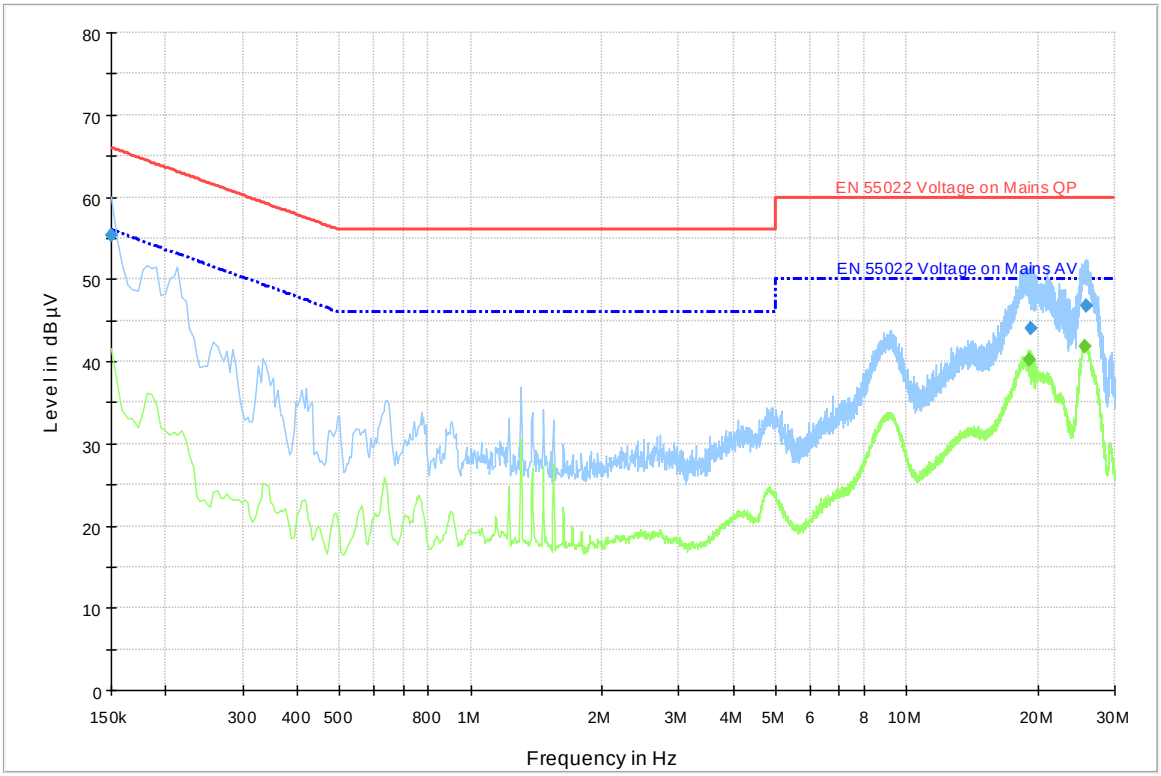

Figure 72 – Conducted Emissions: 115VAC Input.
Output GND connected to ground plane.

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Final Measurement Quasi Peak Detector.

Frequency (MHz)	QuasiPeak (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
0.150000	55.3	1000.000	10.000	On	N	20.0	10.7	66.0	
19.243000	44.0	1000.000	10.000	On	L1	20.0	16.0	60.0	
25.831000	46.7	1000.000	10.000	On	L1	20.0	13.3	60.0	

Table 12 - Conducted Emissions-Quasi Peak Detector: 115VAC Input.

Most Significant Peaks.

Final Measurement Average Detector.

Frequency (MHz)	Average (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
19.036000	40.2	1000.000	10.000	On	N	20.0	9.8	50.0	
25.565500	41.8	1000.000	10.000	On	N	20.0	8.2	50.0	

Table 13 - Conducted Emissions-Average Detector: 115VAC Input.

Most Significant Peaks.

13.2 230VAC

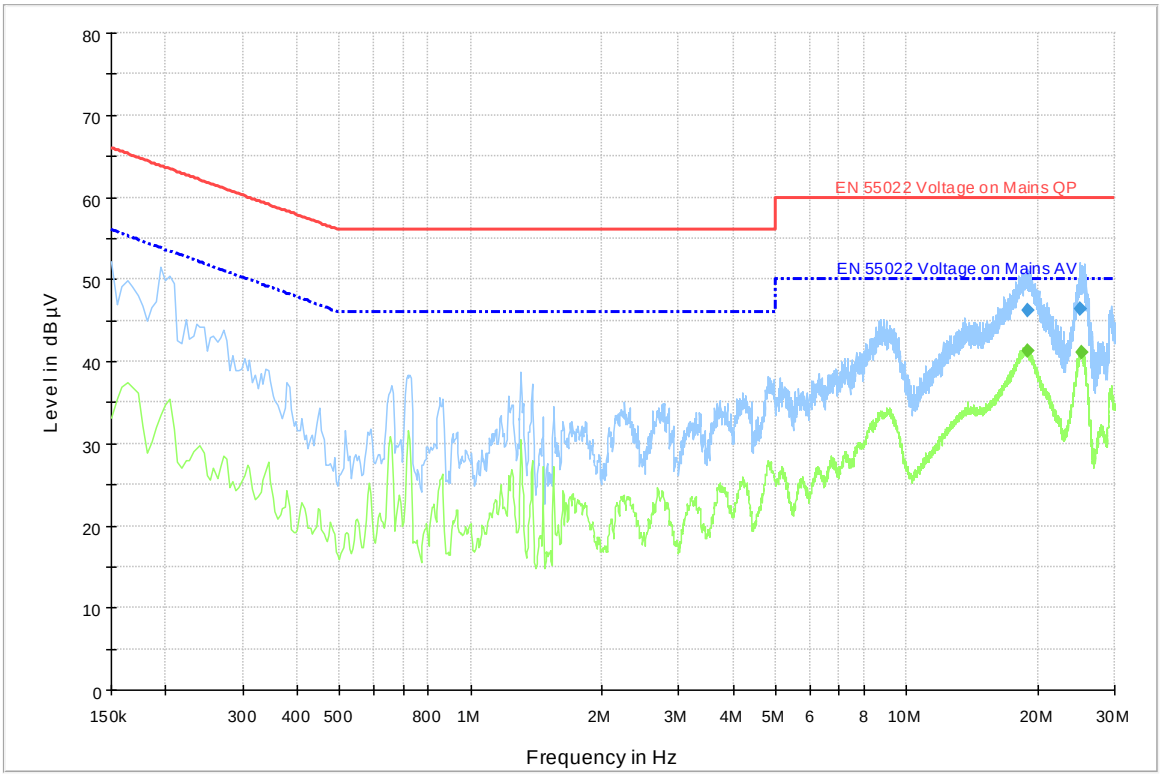

Figure 73 – Conducted Emissions: 230VAC Input.
Output GND connected to ground plane.

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Final Measurement Quasi Peak Detector.

Frequency (MHz)	QuasiPeak (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
18.928000	46.2	1000.000	10.000	On	N	20.0	13.8	60.0	
25.075000	46.4	1000.000	10.000	On	N	20.0	13.6	60.0	

Table 14 - Conducted Emissions- Quasi Peak Detector: 230VAC Input.

Most Significant Peaks.

Final Measurement Average Detector.

Frequency (MHz)	Average (dBµV)	Meas. Time (ms)	Bandwidth (kHz)	Filter	Line	Corr. (dB)	Margin (dB)	Limit (dBµV)	Comment
18.928000	41.3	1000.000	10.000	On	L1	20.0	8.8	50.0	
25.116500	41.1	1000.000	10.000	On	N	20.0	8.9	50.0	

Table 15 - Conducted Emissions- Average Detector: 230VAC Input.

Most Significant Peaks.

14 Lighting Surge Test

14.1 Differential Surge Test

Passed ±1 kV Differential Test.

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

Table 16 - Differential Surge Test Results

14.2 Common mode Surge Test

Passed ±2 kV, CM Surge Test.

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+2	0	L1, L2 / PE	12	10	PASS
-2	0	L1, L2 / PE	12	10	PASS
+2	90	L1, L2 / PE	12	10	PASS
-2	90	L1, L2 / PE	12	10	PASS
+2	180	L1, L2 / PE	12	10	PASS
-2	180	L1, L2 / PE	12	10	PASS
+2	270	L1, L2 / PE	12	10	PASS
-2	270	L1, L2 / PE	12	10	PASS

Table 17 - Common Mode Surge Test Results

14.3 Ring Wave Surge Test Results

Passed ±6 kV, Ring Wave Test

Ring Wave Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+6	0	L1, L2 / PE	12	10	PASS
-6	0	L1, L2 / PE	12	10	PASS
+6	90	L1, L2 / PE	12	10	PASS
-6	90	L1, L2 / PE	12	10	PASS
+6	180	L1, L2 / PE	12	10	PASS
-6	180	L1, L2 / PE	12	10	PASS
+6	270	L1, L2 / PE	12	10	PASS
-6	270	L1, L2 / PE	12	10	PASS

Table 18 - Ring Wave Surge Test Results

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15 ESD Test Results

Load = 5 V 3 A, 38 V 630 mA 38.9 W total.

Supply Voltage=	115VAC		Supply Voltage=	115VAC	
Air discharge	P/F	Comments	Contact discharge	P/F	Comments
+2kV	P		+2kV	P	
-2kV	P		-2kV	P	
+4kV	P		+4kV	P	
-4kV	P		-4kV	P	
+8kV	P		+6kV	P	
-8kV	P		-6kV	P	
+15kV	P		+8kV	P	
-15kV	P		-8kV	P	
Extended Levels			Extended Levels		
16.5kV	P				

Table 19 - ESD Immunity Test Results, 115VAC

Supply Voltage=	230VAC		Supply Voltage=	230VAC	
Air discharge	P/F	Comments	Contact discharge	P/F	Comments
+2kV	P		+2kV	P	
-2kV	P		-2kV	P	
+4kV	P		+4kV	P	
-4kV	P		-4kV	P	
+8kV	P		+6kV	P	
-8kV	P		-6kV	P	
+15kV	P		+8kV	P	
-15kV	P		-8kV	P	
Extended Levels			Extended Levels		
16.5kV	P				

Table 20 - ESD Immunity Test Results, 230VAC

16 Thermals and heatsink design

16.1 Board with Heat Sink

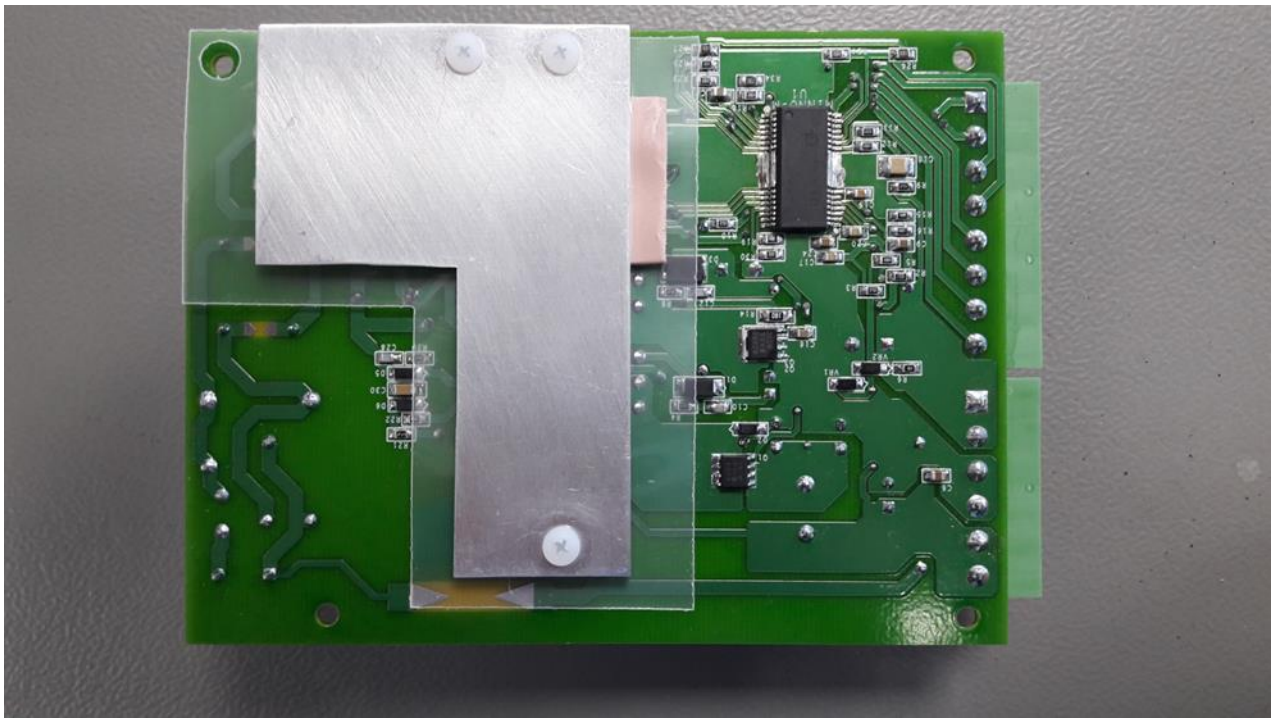

Figure 74 – Populated Circuit Board Photograph, with Heat Sink.

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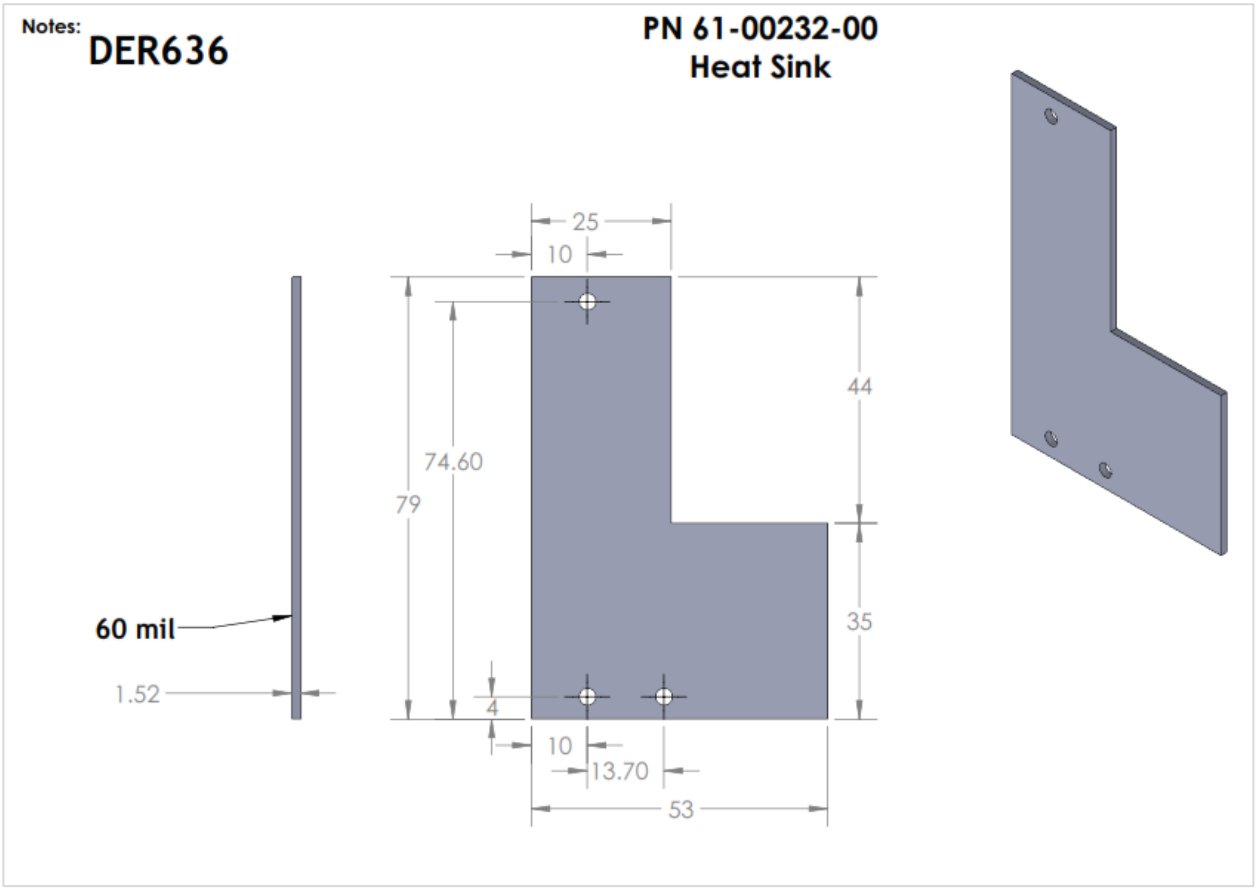
16.2 Component Temperatures with Heat Sink

			Heat sink horizontal facing up					
			90 VAC			265 VAC		Temperature
Component	**Description**	**T1**	**Ambient**	**Delta**	**T1**	**Ambient**	**Delta**	**sensor**
U2	InnoSwitch3-MX	61	25	36	63	25	38	Thermocouple
U1	InnoMux	55.5	25	30.5	55.4	25	30.4	Thermocouple
Q1	SR FET	58.5	25	33.5	55.3	25	30.3	IR sensor
L1	LF CMC Windings	64.2	25	39.2	43.3	25	18.3	IR sensor
L1	LF CMC Core	51	25	26	35	25	10	IR sensor
C3	Bulk Capacitor	47.7	25	22.7	41.5	25	16.5	IR sensor
BR1	Bridge Rectifier	61	25	36	51.2	25	26.2	IR sensor
T1	Transformer Core	57.5	25	32.5	49.7	25	24.7	Thermocouple
			Heat sink vertical-Ac input on bottom edge					
			90 VAC			265 VAC		Temperature
Component	**Description**	**T1**	**Ambient**	**Delta**	**T1**	**Ambient**	**Delta**	**sensor**
U2	InnoSwitch3-MX	56	25	31	61	25	36	Thermocouple
U1	InnoMux	55.1	25	30.1	52.5	25	27.5	Thermocouple
Q1	SR FET	58.2	25	33.2	55.5	25	30.5	IR sensor
L1	LF CMC Windings	64.3	25	39.3	62.5	25	37.5	IR sensor
L1	LF CMC Core	49.3	25	24.3	48	25	23	IR sensor
C3	Bulk Capacitor	47.2	25	22.2	44.7	25	19.7	IR sensor
BR1	Bridge Rectifier	61.2	25	36.2	58	25	33	IR sensor
T1	Transformer Core	56.9	25	31.9	54.5	25	29.5	Thermocouple
			Heat sink horizontal facing down					
						265 VAC		Temperature
					T1	**Ambient**	**Delta**	**sensor**
U2	InnoSwitch3-MX				62	24	38	Thermocouple

Table 21 - Component Temperatures

16.3 Heat Sink Drawing



Material: 3003 Aluminum 60 mil

Figure 75 – Heat Sink Drawing.

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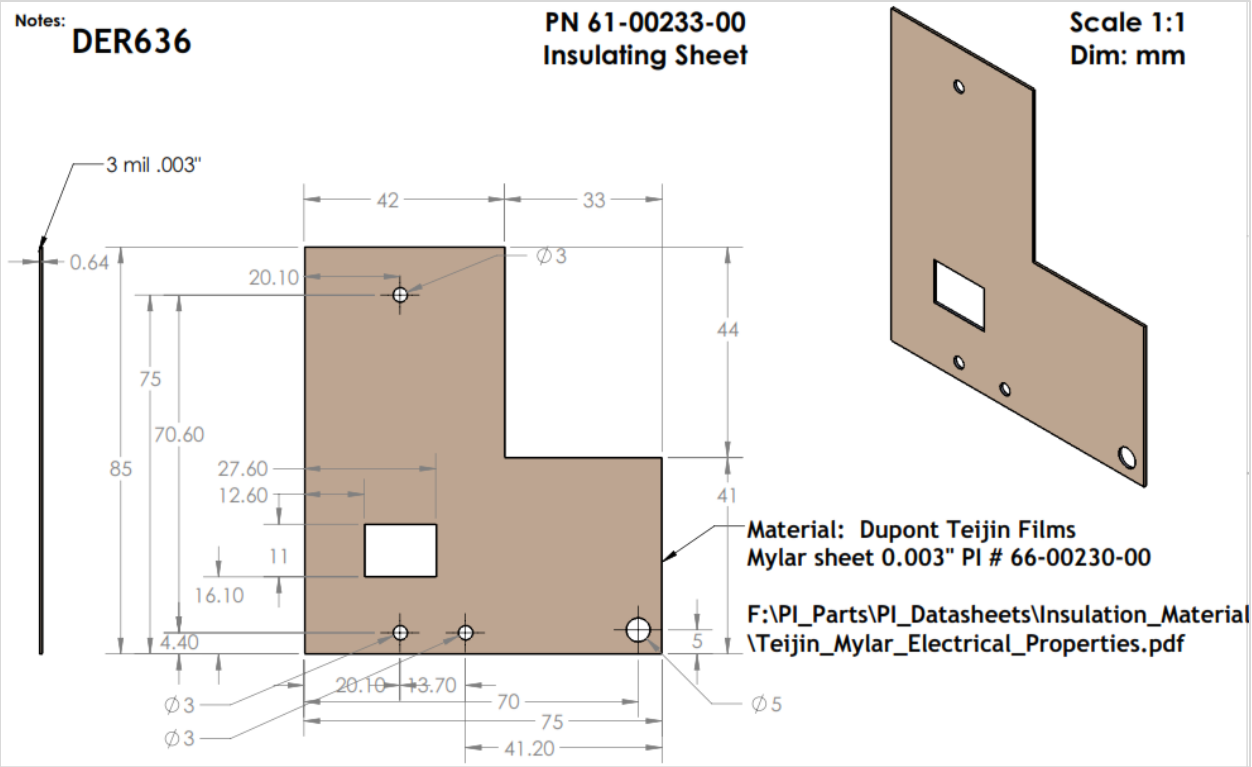
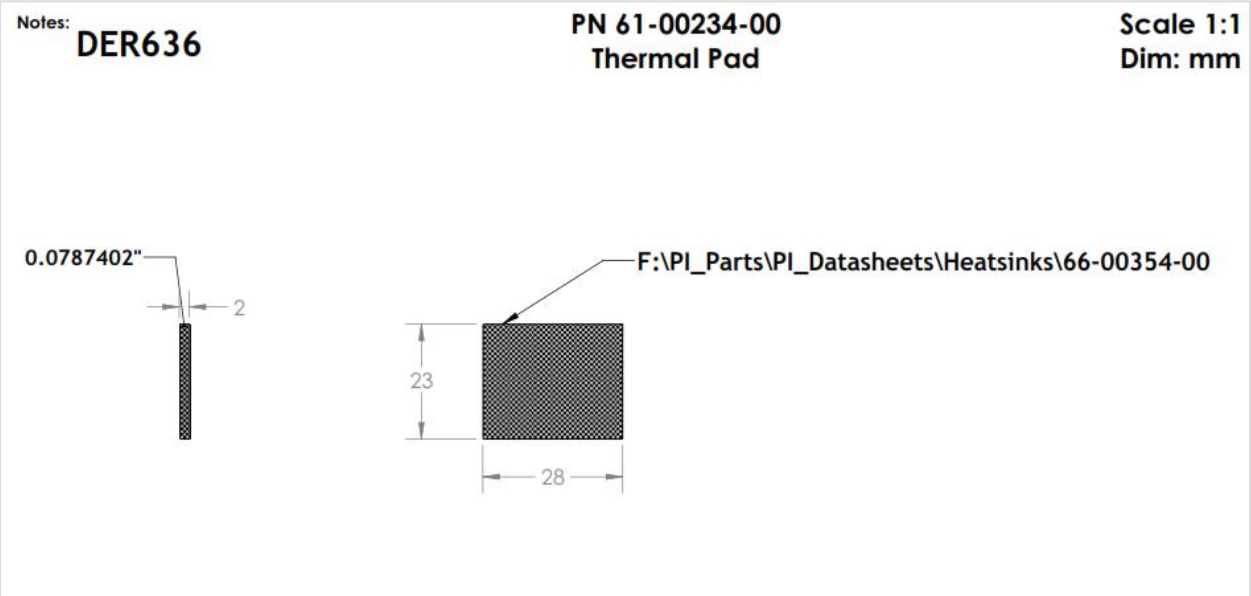
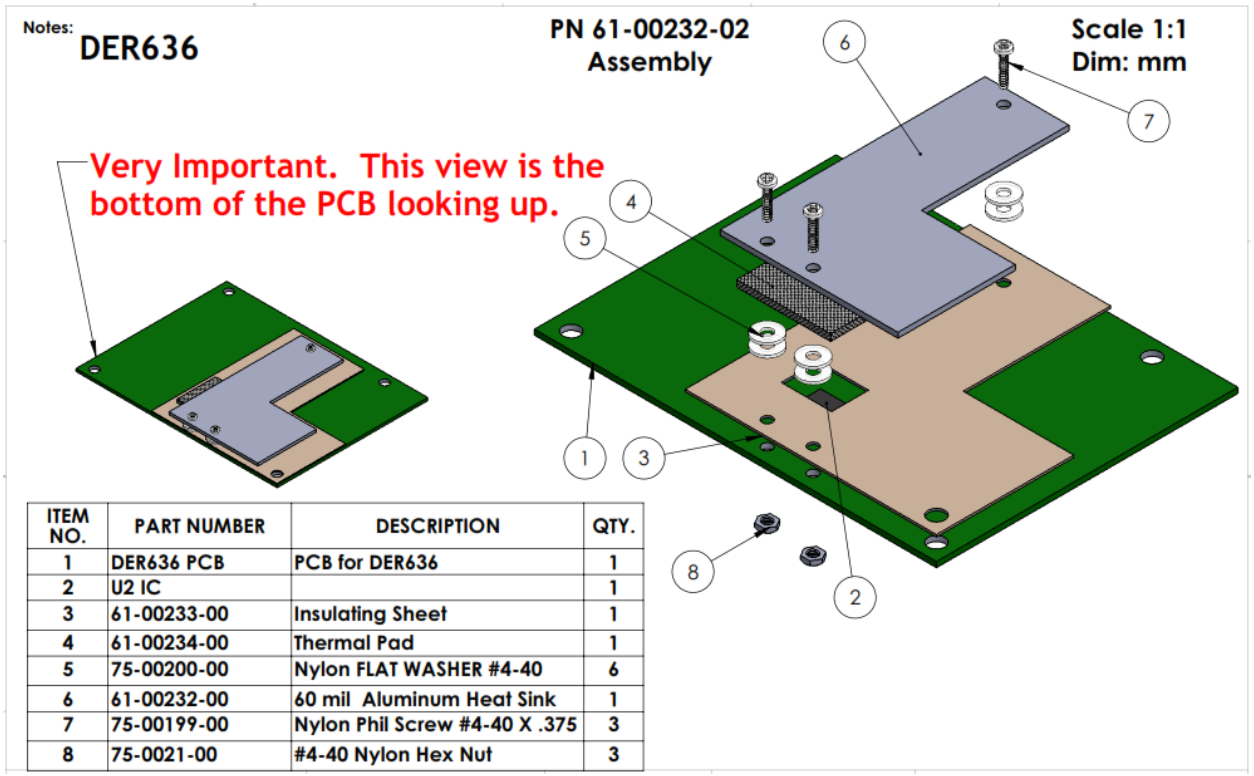


Figure 76 – Heat Sink Insulator Sheet Drawing.



Material: Non-Silicon Pad – t-Global Technology – PC94-150-150-2.0-0

Figure 77 – Heat Sink Thermal Pad Drawing.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	DER636 PCB	PCB for DER636	1
2	U2 IC		1
3	61-00233-00	Insulating Sheet	1
4	61-00234-00	Thermal Pad	1
5	75-00200-00	Nylon FLAT WASHER #4-40	6
6	61-00232-00	60 mil Aluminum Heat Sink	1
7	75-00199-00	Nylon Phil Screw #4-40 X .375	3
8	75-0021-00	#4-40 Nylon Hex Nut	3

Figure 78 – Heat Sink Assembly Drawing.

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17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
19-Mar-19	GBP	1.0	Initial Release	Apps & MKtg
19-Aug-19	GBP	1.1	Updated Pg 17, #5, Figures 19-21 and 28-30.	Apps & MKtg
09-Sept-19	GBP	1.2	Added Table references and index	

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